Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 16K Bytes of In-System Self-Programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 512 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 1K Byte Internal SRAM
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels in TQFP Package Only
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, and 44-pad MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega16L
  - 4.5 - 5.5V for ATmega16
- Speed Grades
  - 0 - 8 MHz for ATmega16L
  - 0 - 16 MHz for ATmega16

8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

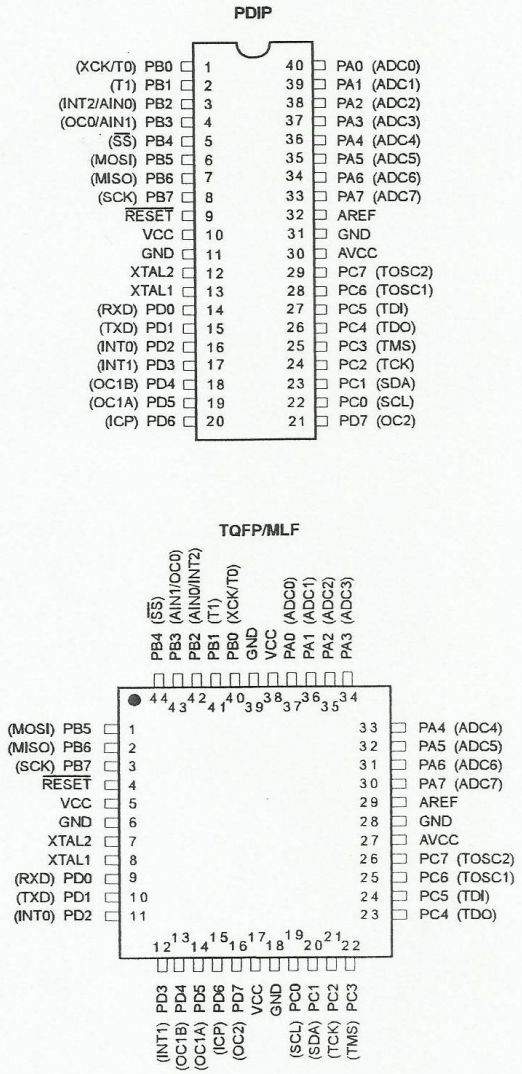
ATmega16
ATmega16L

Preliminary

Rev. 2466E–AVR–10/02

Pin Configurations

Figure 1. Pinouts ATmega16



Disclaimer

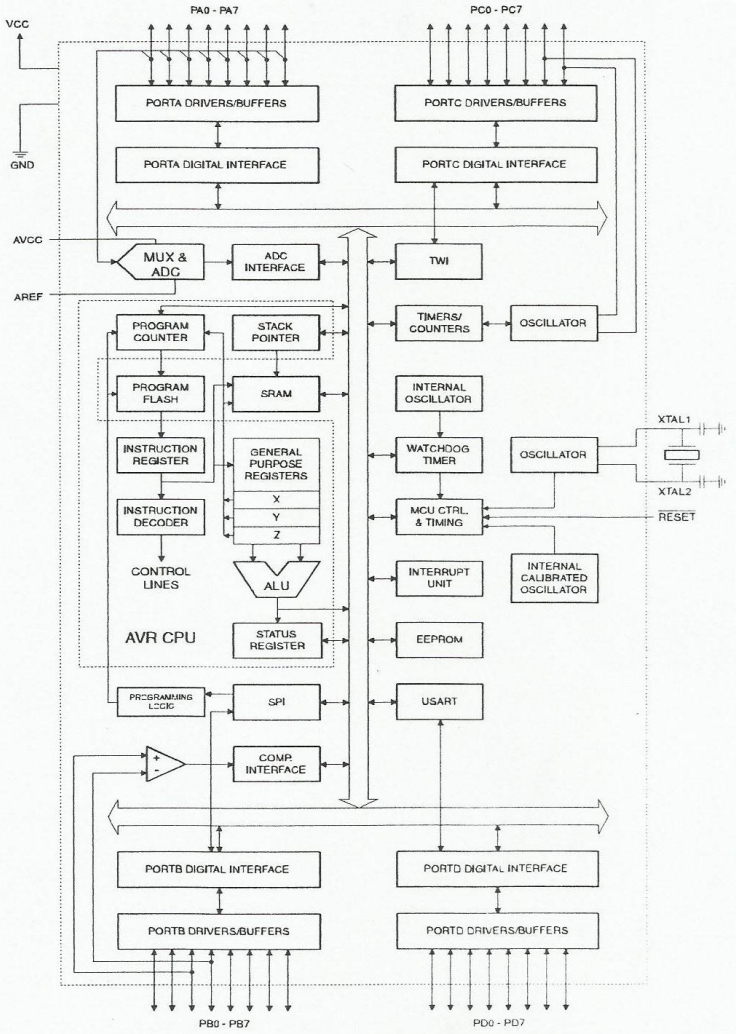
Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Overview

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega16 provides the following features: 16K bytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1K byte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega16 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega16 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC

Digital supply voltage.

GND

Ground.

Port A (PA7..PA0)

Port A serves as the analog inputs to the A/D Converter.

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega16 as listed on page 55.

Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5(TDI), PC3(TMS) and PC2(TCK) will be activated even if a reset occurs.

Port C also serves the functions of the JTAG interface and other special features of the ATmega16 as listed on page 58.

Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega16 as listed on page 60.

$\overline{\text{RESET}}$

Reset Input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 35. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting Oscillator amplifier.

AVCC

AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

AREF

AREF is the analog reference pin for the A/D Converter.

About Code Examples

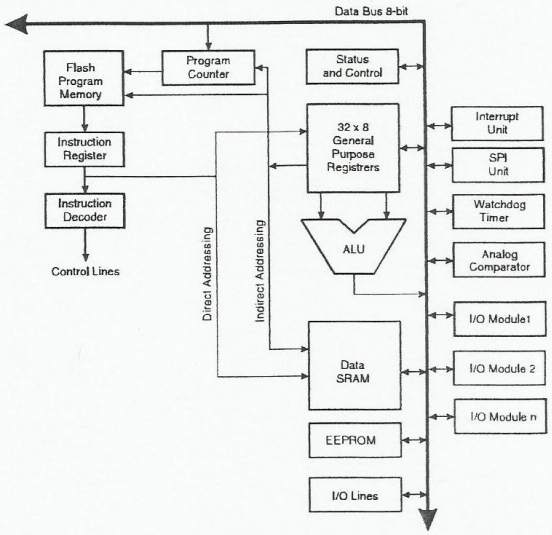
This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C Compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C Compiler documentation for more details.

Introduction

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

Architectural Overview

Figure 3. Block Diagram of the AVR MCU Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory.

The fast-access Register file contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register file, the operation is executed, and the result is stored back in the Register file – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of the these address pointers can also be used as an address pointer for look up tables in Flash Program memory. These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After

an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

Program Flash memory space is divided in two sections, the Boot program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot Program section.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The Stack Pointer SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the Status Register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, SPI, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the Register file, $20 - $5F.

ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format. See the "Instruction Set" section for a detailed description.

Status Register

The Status Register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the Status Register is updated after all ALU operations, as specified in the Instruction Set Reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt. This must be handled by software.

The AVR Status Register – SREG – is defined as:

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the instruction set reference.

- **Bit 6 – T: Bit Copy Storage**

The Bit Copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source or destination for the operated bit. A bit from a register in the Register file can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the Register file by the BLD instruction.

- **Bit 5 – H: Half Carry Flag**

The Half Carry Flag H indicates a half carry in some arithmetic operations. Half Carry is useful in BCD arithmetic. See the "Instruction Set Description" for detailed information.

- **Bit 4 – S: Sign Bit, S = N ⊕ V**

The S-bit is always an exclusive or between the negative flag N and the two's complement overflow flag V. See the "Instruction Set Description" for detailed information.

- **Bit 3 – V: Two's Complement Overflow Flag**

The Two's Complement Overflow Flag V supports two's complement arithmetics. See the "Instruction Set Description" for detailed information.

- **Bit 2 – N: Negative Flag**

The Negative Flag N indicates a negative result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 1 – Z: Zero Flag**

The Zero Flag Z indicates a zero result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 0 – C: Carry Flag**

The Carry Flag C indicates a carry in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

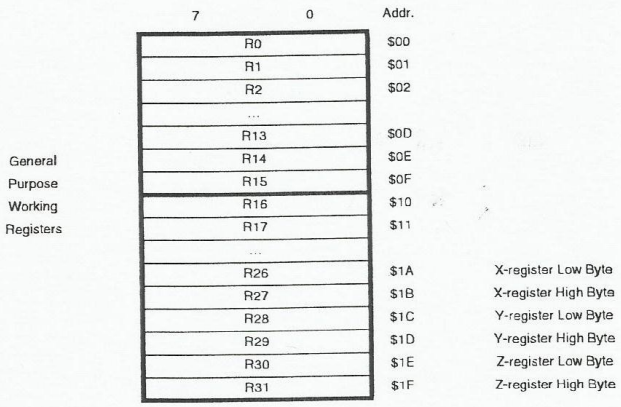
General Purpose Register File

The Register File is optimized for the AVR Enhanced RISC instruction set. In order to achieve the required performance and flexibility, the following input/output schemes are supported by the Register file:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Figure 4 shows the structure of the 32 general purpose working registers in the CPU.

Figure 4. AVR CPU General Purpose Working Registers



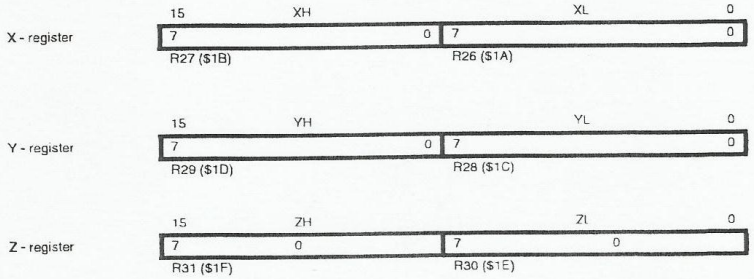
Most of the instructions operating on the Register File have direct access to all registers, and most of them are single cycle instructions.

As shown in Figure 4, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-pointer Registers can be set to index any register in the file.

The X-register, Y-register and Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are 16-bit address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y, and Z are defined as described in Figure 5.

Figure 5. The X-, Y-, and Z-registers



In the different addressing modes these address registers have functions as fixed displacement, automatic increment, and automatic decrement (see the Instruction Set Reference for details).

Stack Pointer

The Stack is mainly used for storing temporary data, for storing local variables and for storing return addresses after interrupts and subroutine calls. The Stack Pointer Register always points to the top of the stack. Note that the stack is implemented as growing from higher memory locations to lower memory locations. This implies that a stack PUSH command decreases the Stack Pointer.

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt Stacks are located. This Stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above $60. The Stack Pointer is decremented by one when data is pushed onto the Stack with the PUSH instruction, and it is decremented by two when the return address is pushed onto the Stack with subroutine call or interrupt. The Stack Pointer is incremented by one when data is popped from the Stack with the POP instruction, and it is incremented by two when data is popped from the Stack with return from subroutine RET or return from interrupt RETI.

The AVR Stack Pointer is implemented as two 8-bit registers in the I/O space. The number of bits actually used is implementation dependent. Note that the data space in some implementations of the AVR architecture is so small that only SPL is needed. In this case, the SPH Register will not be present.

Bit	15	14	13	12	11	10	9	8	
	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SPH
	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

PARALLAX

Web Site: www.parallax.com
Forums: forums.parallax.com
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Office: (916) 624-8333
Fax: (916) 624-8003
Sales: (888) 512-1024
Tech Support: (888) 997-8267

PIR Sensor (#555-28027)

General Description

The PIR (Passive Infra-Red) Sensor is a pyroelectric device that detects motion by measuring changes in the infrared levels emitted by surrounding objects. This motion can be detected by checking for a high signal on a single I/O pin.

Features

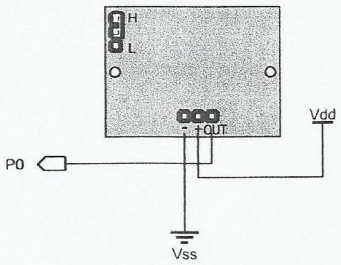
- Single bit output
- Small size makes it easy to conceal
- Compatible with all Parallax microcontrollers
- 3.3V & 5V operation with <100uA current draw

Application Ideas

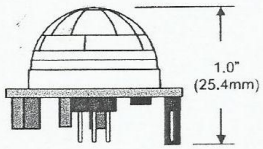
- Alarm Systems
- Halloween Props

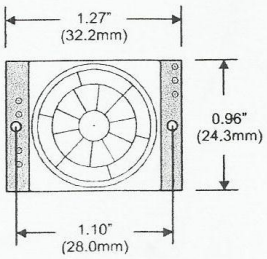
Quick Start Circuit

Note: The sensor is active high when the jumper (shown in the upper left) is in either position.



Module Dimensions





Theory of Operation

Pyroelectric devices, such as the PIR sensor, have elements made of a crystalline material that generates an electric charge when exposed to infrared radiation. The changes in the amount of infrared striking the element change the voltages generated, which are measured by an on-board amplifier. The device contains a special filter called a Fresnel lens, which focuses the infrared signals onto the element. As the ambient infrared signals change rapidly, the on-board amplifier trips the output to indicate motion.

Pin Definitions and Ratings

Pin	Name	Function
-	GND	Connects to Ground or Vss
+	V+	Connects to Vdd (3.3V to 5V) @ ~100uA
OUT	Output	Connects to an I/O pin set to INPUT mode (or transistor/MOSFET)

Jumper Setting

Position	Mode	Description
H	Retrigger	Output remains HIGH when sensor is retriggered repeatedly. Output is LOW when idle (not triggered).
L	Normal	Output goes HIGH then LOW when triggered. Continuous motion results in repeated HIGH/LOW pulses. Output is LOW when idle.

Connecting and Testing

Connect the 3-pin header to your circuit so that the minus (-) pin connects to ground or Vss, the plus (+) pin connects to Vdd and the OUT pin connects to your microcontroller's I/O pin. One easy way to do this would be to use a standard servo/LCD extension cable, available separately from Parallax (#805-00002). This cable makes it easy to plug sensor into the servo headers on our Board Of Education or Professional Development Board. If you use the Board Of Education, be sure the servo voltage jumper (located between the 2 servo header blocks) is in the Vdd position, not Vin. If you do not have this jumper on your board you should manually connect to Vdd through the breadboard. You may also plug the sensor directly into the edge of the breadboard and connect the signals from there. Remember the position of the pins when you plug the sensor into the breadboard.

Calibration

The PIR Sensor requires a 'warm-up' time in order to function properly. This is due to the settling time involved in 'learning' its environment. This could be anywhere from 10-60 seconds. During this time there should be as little motion as possible in the sensors field of view.

Sensitivity

The PIR Sensor has a range of approximately 20 feet. This can vary with environmental conditions. The sensor is designed to adjust to slowly changing conditions that would happen normally as the day progresses and the environmental conditions change, but responds by making its output high when sudden changes occur, such as when there is motion.

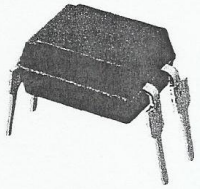
Resources and Downloads

Check out the PIR Sensor product page for example programs and more:

http://www.parallax.com/detail.asp?product_id=555-28027

PC123 Series

DIP 4pin Reinforced Insulation Type Photocoupler



Description

PC123 Series contains an IRED optically coupled to a phototransistor.

It is packaged in a 4-pin DIP, available in wide-lead spacing option and SMT gullwing lead-form option.

Input-output isolation voltage(rms) is 5.0kV.

CTR is 50% to 400% at input current of 5mA.

Features

1. 4-pin DIP package
2. Double transfer mold package (Ideal for Flow Soldering)
3. Current transfer ratio (CTR : MIN. 50% at I_F=5 mA, V_{CE}=5V)
4. Several CTR ranks available
5. Reinforced insulation type (Isolation distance : MIN. 0.4mm)
6. Long creepage distance type (wide lead-form type only : MIN. 8mm)
7. High isolation voltage between input and output ($V_{iso(rms)}$: 5.0 kV)

Agency approvals/Compliance

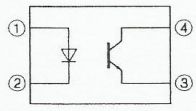
1. Recognized by UL1577 (Double protection isolation), file No. E64380 (as model No. **PC123**)
2. Approved by BSI, BS-EN60065, file No. 7087, BS-EN60950 file No. 7409, (as model No. **PC123**)
3. Approved by SEMCO, EN60065, EN60950, file No. 204582 (as model No. **PC123**)
4. Approved by DEMCO, EN60065, EN60950 (as model No. **PC123**)
5. Approved by NEMKO, EN60065, EN60950, file No. P03100205 (as model No. **PC123**)
6. Approved by FIMKO, EN60065, EN60950, file No. 19383 (as model No. **PC123**)
7. Recognized by CSA file No. CA95323 (as model No. **PC123**)
8. Approved by VDE, VDE0884 (as an option) file No. 83601 or No. 134349 or No.40005304 (as model No. **PC123**)
9. Package resin : UL flammability grade (94V - 0)

Applications

1. I/O isolation for MCUs (Micro Controller Units)
2. Noise suppression in switching circuits
3. Signal transmission between circuits of different potentials and impedances
4. Over voltage detection

Sheet No.: D2-A02902EN
Date Oct. 31, 2003

Internal Connection Diagram

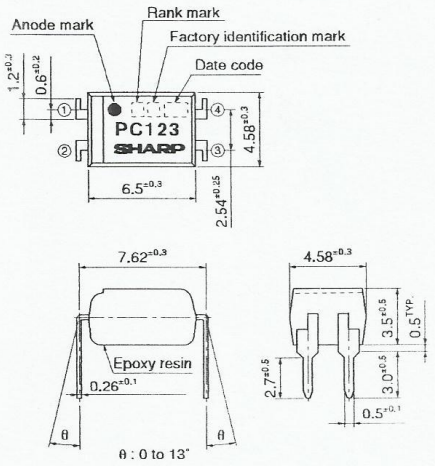


① Anode
② Cathode
③ Emitter
④ Collector

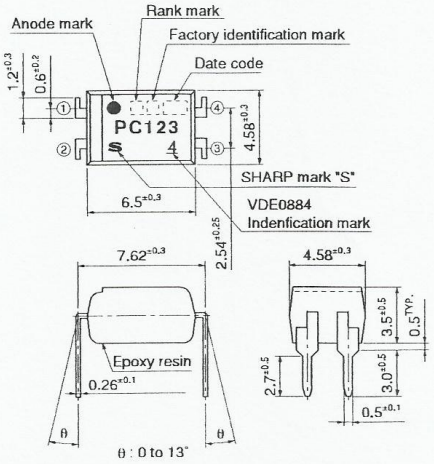
Outline Dimensions

(Unit : mm)

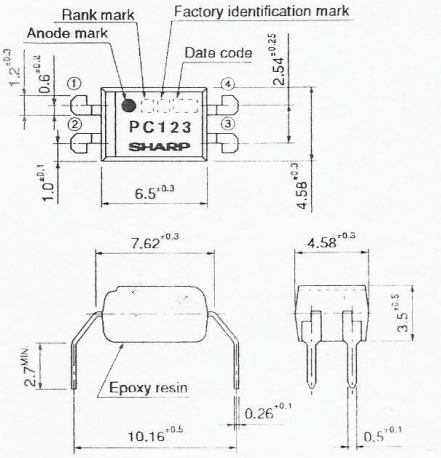
1. Through-Hole [ex. **PC123**]



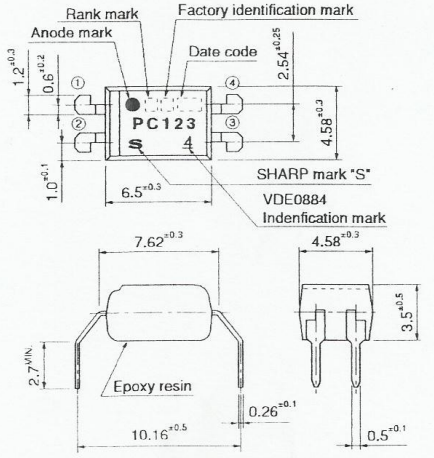
2. Through-Hole (VDE0884 option) [ex. **PC123Y**]



3. Wide Through-Hole Lead-Form [ex. **PC123F**]



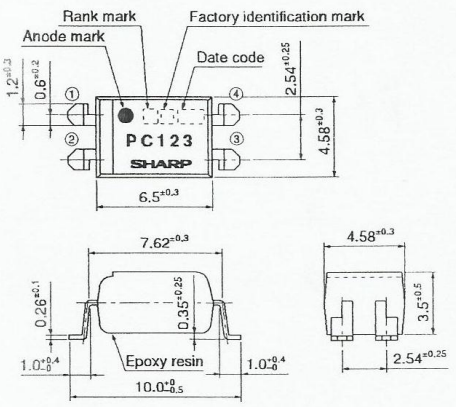
4. Wide Through-Hole Lead-Form (VDE0884 option) [ex. **PC123FY**]



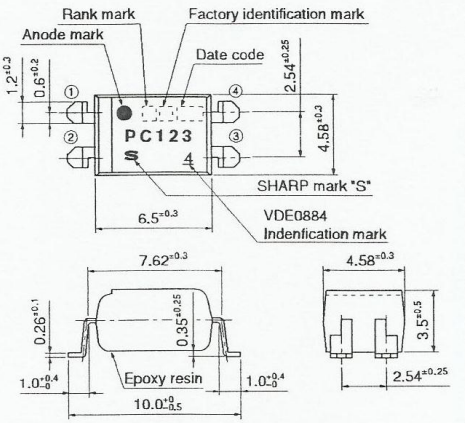
Product mass : approx. 0.18g

(Unit : mm)

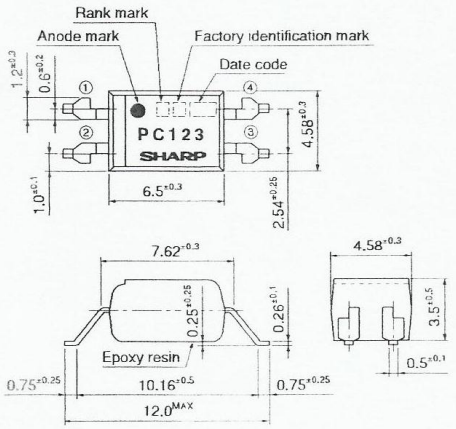
5. SMT Gullwing Lead-Form [ex. **PC123P**]



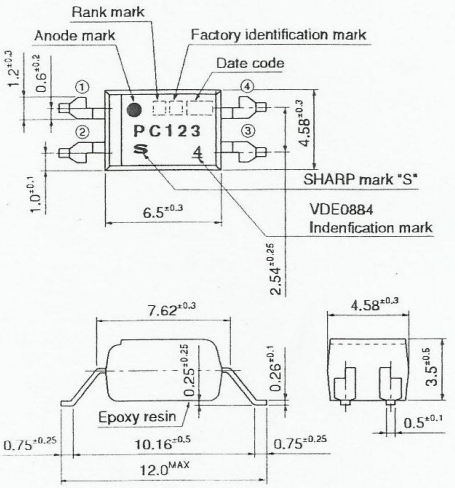
6. SMT Gullwing Lead-Form (VDE0884 option) [ex. **PC123PY**]



7. Wide SMT Gullwing Lead-Form [ex. **PC123FP**]



8. Wide SMT Gullwing Lead-Form (VDE0884 option) [ex. **PC123ZY**]



Product mass : approx. 0.18g

Date code (2 digit)

1st digit				2nd digit	
Year of production				Month of production	
A.D.	Mark	A.D	Mark	Month	Mark
1990	A	2002	P	January	1
1991	B	2003	R	February	2
1992	C	2004	S	March	3
1993	D	2005	T	April	4
1994	E	2006	U	May	5
1995	F	2007	V	June	6
1996	H	2008	W	July	7
1997	J	2009	X	August	8
1998	K	2010	A	September	9
1999	L	2011	B	October	O
2000	M	2012	C	November	N
2001	N	⋮	⋮	December	D

repeats in a 20 year cycle

Factory identification mark

Factory identification Mark	Country of origin
no mark	Japan
■	
◢	Indonesia
▽	Philippines
◥	China

* This factory making is for identification purpose only.
Please contact the local SHARP sales representative to see the actual status of the production.

Rank mark

Refer to the Model Line-up table

Absolute Maximum Ratings

(T_a=25°C)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	*1 Peak forward current	I_{FM}	1	A
	Reverse voltage	V_R	6	V
	Power dissipation	P	70	mW
Output	Collector-emitter voltage	V_{CEO}	70	V
	Emitter-collector voltage	V_{ECO}	6	V
	Collector current	I_C	50	mA
	Collector power dissipation	P_C	150	mW
Total power dissipation		P_{tot}	200	mW
*2 Isolation voltage		$V_{iso\ (rms)}$	5.0	kV
Operating temperature		T_{opr}	−30 to +100	°C
Storage temperature		T_{stg}	−55 to +125	°C
*3 Soldering temperature		T_{sol}	260	°C

*1 Pulse width≤100μs, Duty ratio : 0.001
*2 40 to 60%RH, AC for 1 minute, f = 60Hz
*3 For 10s

Electro-optical Characteristics

(T_a=25°C)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage		V_F	I_F=20mA	–	1.2	1.4	V
	Reverse current		I_R	V_R=4V	–	–	10	μA
	Terminal capacitance		C_t	V=0, f=1kHz	–	30	250	pF
Output	Collector dark current		I_{CEO}	V_{CE}=50V, I_F=0	–	–	100	nA
	Collector-emitter breakdown voltage		BV_{CEO}	I_C=0.1mA, I_F=0	70	–	–	V
	Emitter-collector breakdown voltage		BV_{ECO}	I_E=10μA, I_F=0	6	–	–	nA
Transfer characteristics	Collector current		I_C	I_F=5mA, V_{CE}=5V	2.5	–	20	mA
	Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_F=20mA, I_C=1mA	–	0.1	0.2	V
	Isolation resistance		R_{ISO}	DC500V, 40 to 60%RH	5×10^{10}	1×10^{11}	–	Ω
	Floating capacitance		C_f	V=0, f=1MHz	–	0.6	1.0	pF
	Cut-off frequency		f_c	V_{CE}=5V, I_C=2mA, R_L=100Ω, −3dB	–	80	–	kHz
	Response time	Rise time	t_r	V_{CE}=2V, I_C=2mA, R_L=100Ω	–	4	18	μs
		Fall time	t_f		–	3	18	μs

■ Model Line-up

Lead Form	Through-Hole		Wide Through-Hole		SMT Gullwing		Wide SMT Gullwing		Rank mark	I_C [mA] (I_F=5mA, V_{CE}=5V, T_a=25°C)
Package	Sleeve 100pcs/sleeve				Taping 2 000pcs/reel					
VDE0884	–	Approved	–	Approved	–	Approved	–	Approved		
Model No.	PC123	PC123Y	PC123F	PC123FY	PC123P	PC123PY	PC123FP	PC123ZY	with or without	2.5 to 30.0
	PC123A	PC123Y1	PC123F1	PC123FY1	PC123P1	PC123PY1	PC123FP1	PC123ZY1	A	2.5 to 7.5
	PC123B	PC123Y2	PC123F2	PC123FY2	PC123P2	PC123PY2	PC123FP2	PC123ZY2	B	5.0 to 12.5
	PC123C	PC123Y5	PC123F5	PC123FY5	PC123P5	PC123PY5	PC123FP5	PC123ZY5	No mark	10.0 to 20.0
	PC123S	PC123YS	PC123FS	PC123FY8	PC123PS	PC123PY8	PC123FP8	PC123ZY8	S	5.0 to 10.0

Please contact a local SHARP sales representative to inquire about production status and Lead-Free options.

Fig.1 Forward Current vs. Ambient Temperature

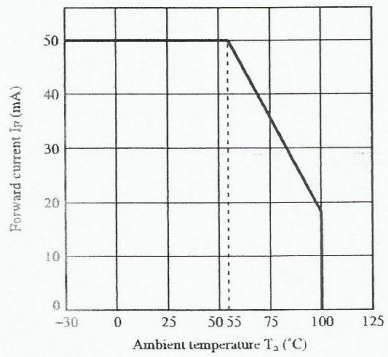


Fig.2 Diode Power Dissipation vs. Ambient Temperature

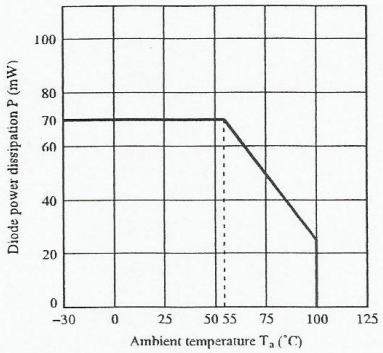


Fig.3 Collector Power Dissipation vs. Ambient Temperature

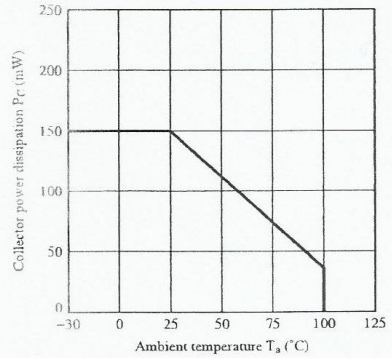


Fig.4 Total Power Dissipation vs. Ambient Temperature

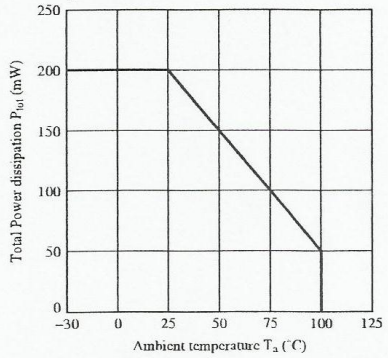


Fig.5 Peak Forward Current vs. Duty Ratio

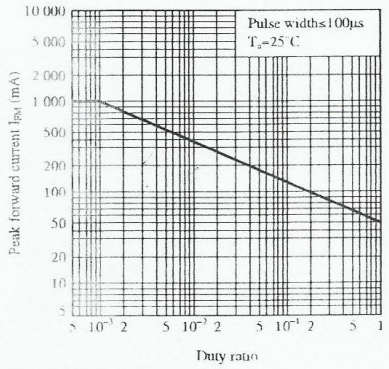


Fig.6 Forward Current vs. Forward Voltage

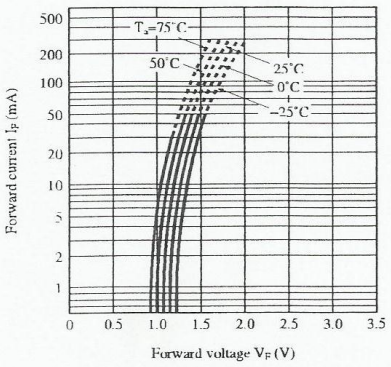


Fig.7 Current Transfer Ratio vs. Forward Current

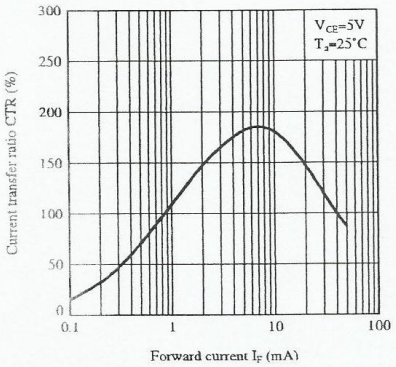


Fig.8 Collector Current vs. Collector-emitter Voltage

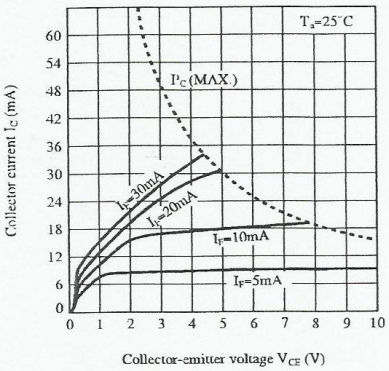


Fig.9 Relative Current Transfer Ratio vs. Ambient Temperature

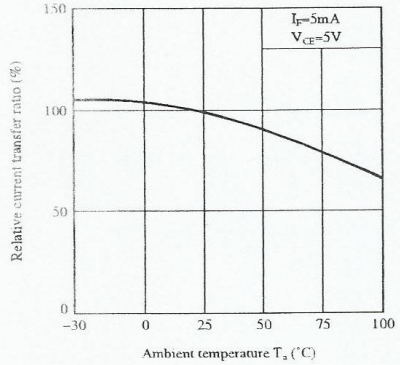


Fig.10 Collector - emitter Saturation Voltage vs. Ambient Temperature

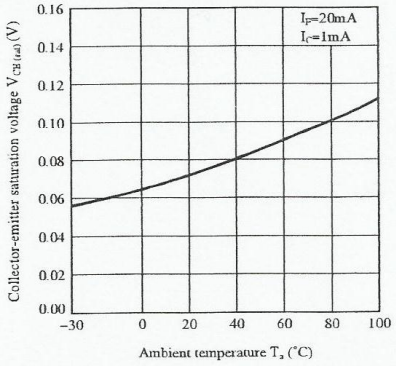


Fig.11 Collector Dark Current vs. Ambient Temperature

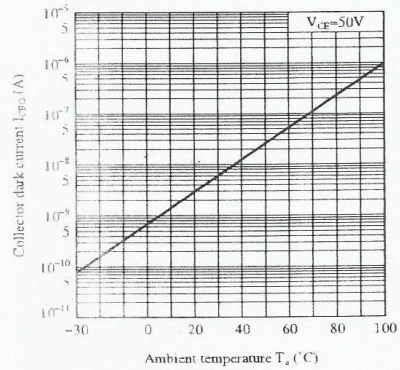


Fig.12 Response Time vs. Load Resistance

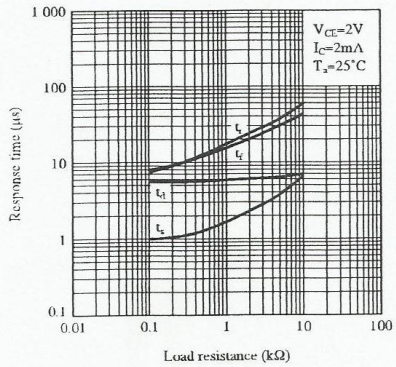
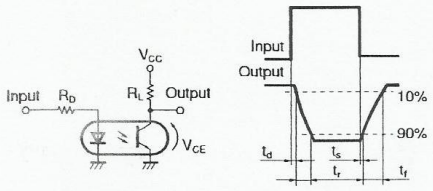


Fig.13 Test Circuit for Response Time



Please refer to the conditions in Fig.12.

Fig.14 Frequency Response

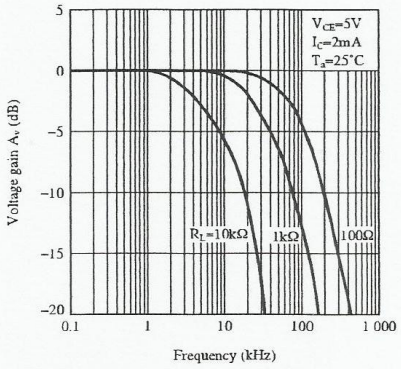
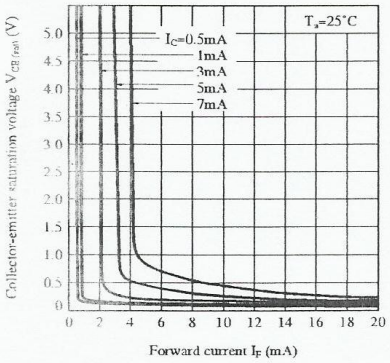


Fig.15 Collector-emitter Saturation Voltage vs. Forward Current



Remarks : Please be aware that all data in the graph are just for reference and not for guarantee.

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Website : www.polisriwijaya.ac.id **E-mail :** info@polsri.ac.id

PELAKSANAAN REVISI LAPORAN AKHIR

Mahasiswa berikut,

Nama	:	Putri Ningrum Pratiwi
NIM	:	061330330285
Jurusan/Program Studi	:	T. Elektro/ T. Telekomunikasi
Judul Laporan Akhir	:	Rancang Bangun Lampu Otomatis Sensor Gerak Menggunakan PIR (*Passive Infrared Receiver* dengan SMS (*Short Message Servie*)

Telah melaksanakan revisi terhadap Laporan Akhir yang diujikan pada hari Kamis tanggal 4 bulan Agustus tahun 2016. Pelaksanaan revisi terhadap Laporan Akhir tersebut telah disetujui oleh Dosen Penguji yang memberikan revisi:

No.	Komentar	Nama Dosen Penguji *)	Tanggal	Tanda Tangan
1.	ace.	DR. Dipl. Ing. Ahmad Taqwa, M.T NIP 196812041997031001	10/8	
2.	Sudah direvisi	Ciksadan,S.T.M.Kom NIP. 196809071993031003	10/08	
3.	Acc	Hj. Emilia Hesti, S.T., M.Kom. NIP. 1972 05271998022001	11/08 16	
4.	Acc	Hj. Adewasti, S.T., M.Kom. NIP.1972 01142001122001	18/08 2016	18/08 2016
5.	Acc	Sopian Soim, S.T.M.T NIP. 197103142001121001	9/2016 08	
6.	Acc	Rosita Febriani.S.T.,M.kom NIP. 197902012003122003	20/08-16	
7.	Acc	Asriyadi,S.T.,M.T NIP. 198404272015041003	10/8-2016	

Palembang, Agustus 2016
Ketua Penguji **),

Rosita Febriani.S.T.,M.kom
NIP. 197902012003122003

Catatan:
*) Dosen penguji yang memberikan revisi saat ujian laporan akhir.
**) Dosen penguji yang ditugaskan sebagai Ketua Penguji saat ujian LA.
Lembaran pelaksanaan revisi ini harus dilampirkan dalam Laporan Akhir.

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KESEPAKATAN BIMBINGAN LAPORAN AKHIR (LA)

Kami yang bertanda tangan di bawah ini,

Pihak Pertama

Nama	: Putri Ningrum Pratiwi
NIM	: 061330330285
Jurusan	: Teknik Elektro
Program Studi	: Teknik Telekomunikasi

Pihak Kedua

Nama	: Martinus Mujur Rose,S.T.,M.T
NIP	: 197412022008121002
Jurusan	: Teknik Elektro
Program Studi	: Teknik Telekomunikasi

Pada hari ini senin dan selasa tanggal 21 Maret 2016 telah sepakat untuk melakukan konsultasi bimbingan Laporan Akhir.

Konsultasi bimbingan sekurang-kurangnya 1 (satu) kali dalam satu minggu. Pelaksanaan bimbingan pada setiap hari senin dan selasa pukul 15.10, tempat di Politeknik Negeri Sriwijaya.

Demikianlah kesepakatan ini dibuat dengan penuh kesadaran guna kelancaran penyelesaian Laporan Akhir.

Palembang, 21 Maret 2016

Pihak Pertama,

(Putri Ningrum Pratiwi)
NIM 061330330285

Pihak Kedua,

(Martinus Mujur Rose,S.T.,M.T)
NIP 197412022008121002

Mengetahui,
Ketua Jurusan

(Yudi Wijanarko,S.T.,M.T)
NIP 196705111992031003

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KESEPAKATAN BIMBINGAN LAPORAN AKHIR (LA)

Kami yang bertanda tangan di bawah ini,

Pihak Pertama

Nama	: Putri Ningrum Pratiwi
NIM	: 061330330285
Jurusan	: Teknik Elektro
Program Studi	: Teknik Telekomunikasi

Pihak Kedua

Nama	: Rosita Febriani,S.T.,M.Kom
NIP	: 197902012003122003
Jurusan	: Teknik Elektro
Program Studi	: Teknik Telekomunikasi

Pada hari ini kamis dan jumat tanggal 29 April 2016 telah sepakat untuk melakukan konsultasi bimbingan Laporan Akhir.

Konsultasi bimbingan sekurang-kurangnya 1 (satu) kali dalam satu minggu. Pelaksanaan bimbingan pada setiap hari kamis dan jumat pukul 10.00, tempat di Politeknik Negeri Sriwijaya.

Demikianlah kesepakatan ini dibuat dengan penuh kesadaran guna kelancaran penyelesaian Laporan Akhir.

Palembang, 29 April 2016

Pihak Pertama,

(Putri Ningrum Pratiwi)
NIM 061330330285

Pihak Kedua,

(Rosita Febriani,S.T.,M.Kom)
NIP 197902012003122003

Mengetahui,
Ketua Jurusan

(Yudi Wijanarko,S.T.,M.T)
NIP 196705111992031003

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LEMBAR BIMBINGAN LAPORAN AKHIR

Lembar : 1

Nama : Putri Ningrum Pratiwi
NIM : 061330330285
Jurusan/Program Studi : Teknik Elektro/ Teknik Telekomunikasi
Judul Laporan Akhir : Rancang Bangun Lampu Otomatis Sensor Gerak Menggunakan PIR (*Passive Infrared Receiver*) Dengan SMS (*Short Message Service*)
Pembimbing I / II *) : Martinus Mujur Rose,S.T.,M.T

No.	Tanggal	Uraian Bimbingan	Tanda Tangan Pembimbing
1.	9/6-2016	Bab I. Topik / judul. → Revisi.	
2.	10/6-2016	Bab I & II. → Perbaikan tata penulisan	
3.	13/6-2016	Bab I. ACC. → Revisi Bab II (tata penulisan).	
4.	15/6-2016	Bab II. ACC. Lanjutkan Bab III.	
5.	20/6-2016	Bab III. Perbaiki Flowchart.	
6.	21/6-2016	Bab IV. Revisi. Bab III. Acc.	
7.	24/6-2016	Bab IV. Perbaiki nama Tabel.	

No.	Tanggal	Uraian Bimbingan	Tanda Tangan Pembimbing
8.	28/6-2016	- Bab IV. Perbaiki tata tulis menjelaskan rujukan. (cth: analisa – analisis), dll.	
9.	14/7-2016	- Acc. Bab IV. → Lanjutkan Bab V.	
10.	15/7-2016	→ Perbaiki kesimpulan no. 4.	
11.	19/7-2016	→ Perbaiki saran.	
12.	22/7-2016	→ ACC. (siap Ujian Skripsi).	

Palembang, Juni

Ketua Jurusan/KPS,

(Ciksadan, S.T.,M.Kom)
NIP 196809071993031003

Catatan:
*) melingkari angka yang sesuai.
Ketua Jurusan/Ketua Program Studi harus memeriksa jumlah pelaksanaan bimbingan sesuai yang dipersyaratkan dalam Pedoman Laporan Akhir sebelum menandatangani lembar bimbingan ini.
Lembar pembimbingan LA ini harus dilampirkan dalam Laporan Akhir.

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LEMBAR BIMBINGAN LAPORAN AKHIR

Lembar : 1

Nama : Putri Ningrum Pratiwi
NIM : 061330330285
Jurusan/Program Studi : Teknik Elektro/ Teknik Telekomunikasi
Judul Laporan Akhir : Rancang Bangun Lampu Otomatis Sensor Gerak Menggunakan PIR (*Passive Infrared Receiver*) Dengan SMS (*Short Message Service*)
Pembimbing I / II *) : Rosita Febriani, S.T.,M.Kom

No.	Tanggal	Uraian Bimbingan	Tanda Tangan Pembimbing
1.	15/6-2016	Revisi Bab I : Tata Tulis	
2.	19/6-2016	Revisi Bab II , Acc Bab I	
3.	19/6-2016	Revisi Bab III : Diagram , Flowchart	
4.	22/6-2016	Revisi Bab III : Tata penulisan Program & flowchart	
5.	23/2016 /6	Perhatikan Penulisan/urutan penomoran	
6.	23/2016 /6	Acc Bab III	
7.	11/7-2016	Revisi Bab IV : Perhatikan tata letak halaman	

No.	Tanggal	Uraian Bimbingan	Tanda Tangan Pembimbing
8.	13/7-2016	Acc Bab IV	
9.	15/7-2016	-Acc Bab IV -Revisi Abstrak	
10.	18/7-2016	-Acc Abstrak -Daftar pustaka: Tata cara penulisan	
11.	19/7-2016	Acc : Daftar pustaka	
12.	22/7-2016	Acc siap mengikuti ujian sidang akhir	

Palembang, Juni

Ketua Jurusan/KPS,

(Ciksadan, S.T.,M.Kom)
NIP 196809071993031003

Catatan:
*) melingkari angka yang sesuai.
Ketua Jurusan/Ketua Program Studi harus memeriksa jumlah pelaksanaan bimbingan sesuai yang dipersyaratkan dalam Pedoman Laporan Akhir sebelum menandatangani lembar bimbingan ini.
Lembar pembimbingan LA ini harus dilampirkan dalam Laporan Akhir.

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Website : www.polisriwijaya.ac.id E-mail : info@polsri.ac.id

REKOMENDASI UJIAN LAPORAN AKHIR (LA)

Pembimbing Laporan Akhir memberikan rekomendasi kepada,

Nama	:	Putri Ningrum Pratiwi
NIM	:	061330330285
Jurusan/Program Studi	:	Teknik Elektro/ Teknik Telekomunikasi
Judul Laporan Akhir	:	Rancang Bangun Lampu Otomatis Sensor Gerak Menggunakan PIR (*Passive Infrared Receiver*) Dengan Sms (Short Message Service)

Mahasiswa tersebut telah memenuhi persyaratan dan dapat mengikuti Ujian Laporan Akhir (LA) pada Tahun Akademik 2016

Palembang, Agustus 2016

Pembimbing I,

(Rosita Febriani,S.T.,M.Kom)
NIP 197902012003122003

Pembimbing II,

(Martinus Mujur Rose,S.T.,M.T)
NIP 197412022008121002

Kepada

Yth. Kepala LaboratoriumTeknik Telekomunikasi

di

Tempat

Saya yang bertanda tangan dibawah ini :

Nama	: Putri Ningrum Pratiwi
NIM	: 0613 3033 0285
Kelas	: 6 TB
Judul	: Rancang Bangun Lampu Otomatis Sensor Gerak menggunakan PIR (*Passive Infrared Receover*) dengan SMS (*Short Message Service*)

Dosen pembimbing 1 : Rosita Febriani,S.T.,M.Kom

Dosen Pembimbing 2 : Martinus Mujur Rose,S.T.,M.T

Dengan ini mengajukan permohonan untuk menggunakan laboratorium serta meminjam beberapa peralatan praktikum antara lain :

1. Osiloskop
2. Kabel BNC jepit buaya
3. Multimeter digital
4. Probe Osiloskop
5. Kabel Jumper buaya

Untuk syarat menyelesaikan Laporan Akhir jurusan Teknik Elektro program studi Teknik Telekomunikasi. Dalam kepentingan pengambilan data ini, saya mohon kesediaan Bapak/Ibu pembimbing untuk membimbingi. Demikianlah permohonan ini saya buat sebenar-benarnya. Atas perhatiannya saya ucapkan terimakasih.

Palembang, 22 Juni 2016

METERAI TEMPEL CD313AEF023775761 6000 ENAM RIBU RUPIAH

Putri Ningrum Pratiwi

NPM. 061330330285

No.	Tanggal	Pembimbing I	Pembimbing II	Keterangan
1.	22 Juni 2016			- Uji Coba alat - ambil data.
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				
11.				
12.				
13.				

Mengetahui,

Ketua Program Studi

Ciksadan, S.T., M.Kom
NIP. 196809071993031003

Kepala Lab. Telekomunikasi

Sopian Soim, S.T., M.T
NIP.197103142001121001

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BUKTI PENYERAHAN HASIL KARYA/RANCANG BANGUN

Pada hari ini ..Rabu..... tanggal ..24.. bulan ...Agustus..... tahun ..2016.. telah diserahkan seperangkat karya/rancang bangun kepada Jurusan Teknik Elektro Program Studi Teknik Telekomunikasi di Politeknik Negeri Sriwijaya,

Nama Perangkat	Spesifikasi
LAMPU OTOMATIS SENSOR GERAK MENGGUNAKAN PIR (*PASSIVE INFRARED RECEIVER*) dengan SMS	ATMega16, sensor Pir, Laampu, SMS (Short Message Service)

Hasil karya/rancang bangun dari,

Nama	NIM	Nama Pembimbing
Putri Ningrum Pratiwi	061330330285	Rrosita Febriani. S.T.,M.Kom
		Martinus Mujur Rose,S.T.M.T

Palembang, ...2016

Yang menerima *),

(Sopian Soim, S.T.,M.T)
NIP 197103142001121001

Yang menyerahkan **),

(Putri Ningrum Pratiwi)
NIM 061330330285

Mengetahui,
Ketua Jurusan/KPS,

(Ciksadan,S.T.,M.Kom)
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*) pejabat Jurusan/PS yang ditunjuk (Kepala Lab./Bengkel atau Kepala Seksi)
**) perwakilan mahasiswa dari pembuat karya/rancang bangun.