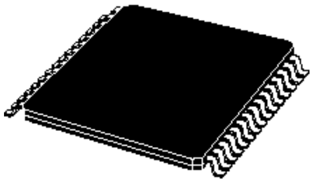
VNH2SP30-E

Automotive fully integrated H-bridge motor driver

Features

Type	$R_{DS(on)}$	I_{out}	V_{ccmax}
VNH2SP30-E	19mΩ max (per leg)	30A	41V

- 5V logic level compatible inputs
- Undervoltage and overvoltage shut-down
- Overvoltage clamp
- Thermal shut down
- Cross-conduction protection
- Linear current limiter
- Very low stand-by power consumption
- PWM operation up to 20 kHz
- Protection against loss of ground and loss of V_{CC}
- Current sense output proportional to motor current
- Package: ECOPACK®



MultiPowerSO-30™

Description

The VNH2SP30-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high side driver and two low side switches. The high side driver switch is designed using STMicroelectronic's well known and proven proprietary VIPower™ M0 technology which permits efficient integration on the same die of a true Power MOSFET with an intelligent signal/protection circuitry.

The low side switches are vertical MOSFETs manufactured using STMicroelectronic's proprietary EHD ('STripFET™') process. The three die are assembled in the MultiPowerSO-30 package on electrically isolated leadframes. This package, specifically designed for the harsh automotive environment offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals IN_A and IN_B can directly interface to the microcontroller to select the motor direction and the brake condition. The $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull-up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The normal condition operation is explained in *Table 12: Truth table in normal operating conditions on page 14*. The motor current can be monitored with the CS pin by delivering a current proportional to its value. The speed of the motor can be controlled in all possible conditions by the PWM up to 20 kHz. In all cases, a low level state on the PWM pin will turn off both the LS_A and LS_B switches. When PWM rises to a high level, LS_A or LS_B turn on again depending on the input pin state.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and Reel
MultiPowerSO-30	VNH2SP30-E	VNH2SP30TR-E

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1 Block diagram and pin description

Figure 1. Block diagram

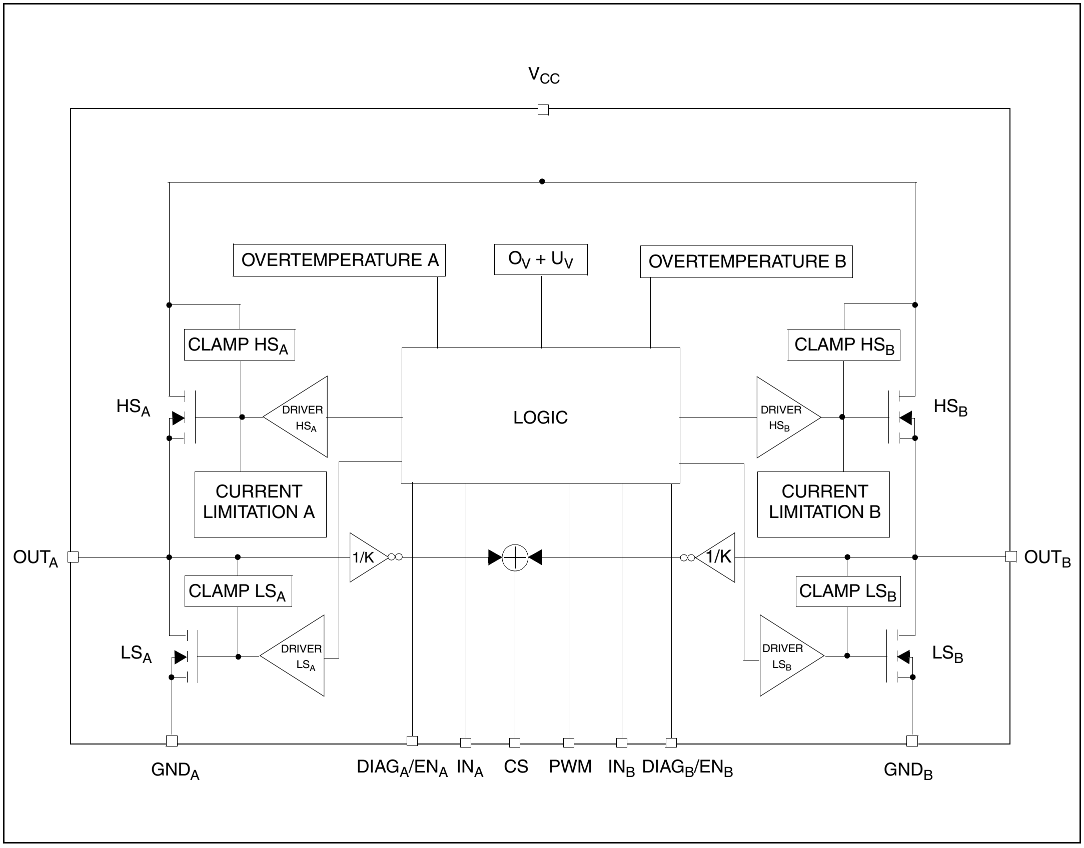


Table 2. Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high side and the low side switches according to the truth table
Overvoltage + undervoltage	Shuts down the device outside the range [5.5V..16V] for the battery voltage
High side and low side clamp voltage	Protects the high side and the low side switches from the high voltage on the battery line in all configurations for the motor
High side and low side driver	Drives the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge
Linear current limiter	Limits the motor current by reducing the high side switch gate-source voltage when short-circuit to ground occurs
Overtemperature protection	In case of short-circuit with the increase of the junction's temperature, shuts down the concerned high side to prevent its degradation and to protect the die
Fault detection	Signals an abnormal behavior of the switches in the half-bridge A or B by pulling low the concerned $EN_x/DIAG_x$ pin

Figure 2. Configuration diagram (top view)

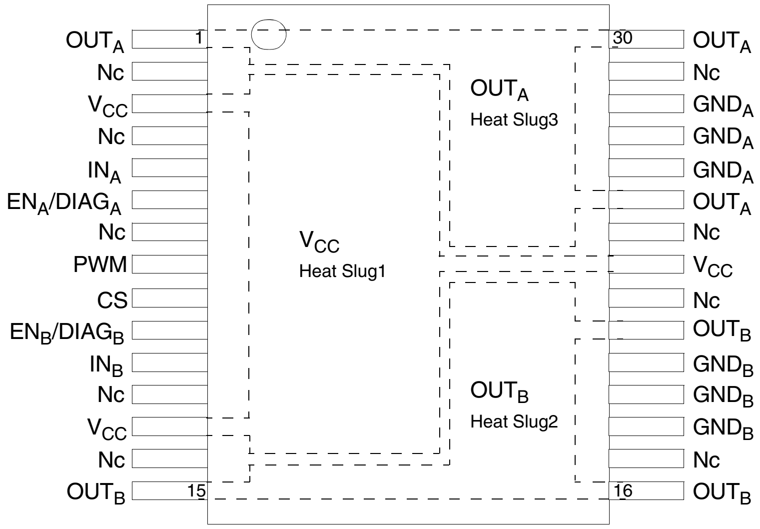


Table 3. Pin definitions and functions

Pin No	Symbol	Function
1, 25, 30	OUT_A, Heat Slug3	Source of high side switch A / Drain of low side switch A
2, 4, 7, 12, 14, 17, 22, 24, 29	NC	Not connected
3, 13, 23	V_{CC}, Heat Slug1	Drain of high side switches and power supply voltage
6	$EN_A/DIAG_A$	Status of high side and low side switches A; open drain output
5	IN_A	Clockwise input
8	PWM	PWM input
9	CS	Output of current sense
11	IN_B	Counter clockwise input
10	$EN_B/DIAG_B$	Status of high side and low side switches B; open drain output
15, 16, 21	OUT_B, Heat Slug2	Source of high side switch B / Drain of low side switch B
26, 27, 28	GND_A	Source of low side switch A(1)
18, 19, 20	GND_B	Source of low side switch B(1)

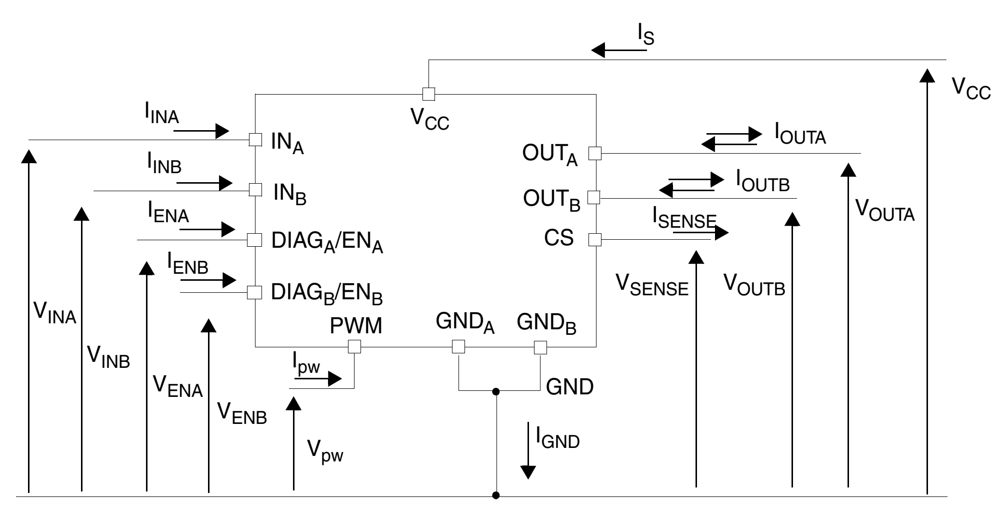
1. GND_A and GND_B must be externally connected together.

Table 4. Pin functions description

Name	Description
V_{CC}	Battery connection
GND_A, GND_B	Power grounds; must always be externally connected together
OUT_A, OUT_B	Power connections to the motor
IN_A, IN_B	Voltage controlled input pins with hysteresis, CMOS compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V_{CC}, brake to GND, clockwise and counterclockwise).
PWM	Voltage controlled input pin with hysteresis, CMOS compatible. Gates of low side FETs are modulated by the PWM signal during their ON phase allowing speed control of the motor.
$EN_A/DIAG_A$, $EN_B/DIAG_B$	Open drain bidirectional logic pins. These pins must be connected to an external pull up resistor. When externally pulled low, they disable half-bridge A or B. In case of fault detection (thermal shutdown of a high side FET or excessive ON state voltage drop across a low side FET), these pins are pulled low by the device (see truth table in fault condition).
CS	Analog current sense output. This output sources a current proportional to the motor current. The information can be read back as an analog voltage across an external resistor.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+41	V
I_{max}	Maximum output current (continuous)	30	A
I_R	Reverse output current (continuous)	-30	
I_{IN}	Input current (IN_A and IN_B pins)	±10	mA
I_{EN}	Enable input current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins)	±10	
I_{pw}	PWM input current	±10	
V_{CS}	Current sense maximum voltage	-3/+15	V
V_{ESD}	Electrostatic discharge (R = 1.5kΩ, C = 100pF) – CS pin – logic pins – output pins: OUT_A, OUT_B, V_{CC}	 2 4 5	 kV kV kV
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	
T_{STG}	Storage temperature	-55 to 150	

2.2 Electrical characteristics

V_{CC} = 9V up to 16 V; -40°C < T_J < 150°C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		5.5		16	V
I_S	Supply current	Off state with all Fault Cleared & ENx=0				
		$IN_A = IN_B = PWM = 0$; $T_j = 25°C$; $V_{CC} = 13V$		12	30	μA
		$IN_A = IN_B = PWM = 0$			60	μA
		Off state: $IN_A = IN_B = PWM = 0$		2		mA
		On state: IN_A or IN_B = 5V, no PWM			10	mA
R_{ONHS}	Static high side resistance	I_{OUT} = 15A; T_j = 25°C			14	mΩ
		I_{OUT} = 15A; T_j = -40 to 150°C			28	
R_{ONLS}	Static low side resistance	I_{OUT} = 15A; T_j = 25°C			5	
		I_{OUT} = 15A; T_j = -40 to 150°C			10	
V_f	High side free-wheeling diode forward voltage	I_f = 15A		0.8	1.1	V
$I_{L(off)}$	High side off state output current (per channel)	T_j = 25°C; $V_{OUTX} = EN_X$ = 0V; V_{CC} = 13V			3	μA
		T_j = 125°C; $V_{OUTX} = EN_X$ = 0V; V_{CC} = 13V			5	
I_{RM}	Dynamic cross-conduction current	I_{OUT} = 15A (see *Figure 7*)		0.7		A

Table 7. Logic inputs (IN_A, IN_B, EN_A, EN_B)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)			1.25	V
V_{IH}	Input high level voltage		3.25			
V_{IHYST}	Input hysteresis voltage		0.5			
V_{ICL}	Input clamp voltage	I_{IN} = 1mA	5.5	6.3	7.5	
		I_{IN} = -1mA	-1.0	-0.7	-0.3	
I_{INL}	Input low current	V_{IN} = 1.25V	1			μA
I_{INH}	Input high current	V_{IN} = 3.25V			10	
V_{DIAG}	Enable output low level voltage	Fault operation ($DIAG_X/EN_X$ pin acts as an output pin); I_{EN} = 1mA			0.4	V

Table 8. PWM

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{pwl}	PWM low level voltage				1.25	V
I_{pwl}	PWM pin current	V_{pw} = 1.25V	1			μA
V_{pwh}	PWM high level voltage		3.25			V
I_{pwh}	PWM pin current	V_{pw} = 3.25V			10	μA
$V_{pwhhyst}$	PWM hysteresis voltage		0.5			V
V_{pwcl}	PWM clamp voltage	I_{pw} = 1mA	V_{CC} + 0.3	V_{CC} + 0.7	V_{CC} + 1.0	
		I_{pw} = -1mA	-6.0	-4.5	-3.0	
C_{INPWM}	PWM pin input capacitance	V_{IN} = 2.5V			25	pF

Table 9. Switching (V_{CC} = 13V, R_{LOAD} = 0.87Ω , unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f	PWM frequency		0		20	kHz
$t_{d(on)}$	Turn-on delay time	Input rise time < 1μs (see *Figure 6*)			250	μs
$t_{d(off)}$	Turn-off delay time	Input rise time < 1μs (see *Figure 6*)			250	
t_r	Rise time	(see *Figure 5*)		1	1.6	
t_f	Fall time	(see *Figure 5*)		1.2	2.4	
t_{DEL}	Delay time during change of operating mode	(see *Figure 4*)	300	600	1800	
t_{rr}	High side free wheeling diode reverse recovery time	(see *Figure 7*)		110		ns
$t_{off(min)}$(1)	PWM minimum off time	9V < V_{CC} < 16V; T_j = 25°C; L = 250μH; I_{OUT} = 15A			6	μs

1. To avoid false Short to Battery detection during PWM operation, the PWM signal must be low for a time longer than 6μs.

Table 10. Protection and diagnostic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{USD}	Undervoltage shut-down				5.5	V
	Undervoltage reset			4.7		
V_{OV}	Overvoltage shut-down		16	19	22	
I_{LIM}	High side current limitation		30	50	70	A
V_{CLP}	Total clamp voltage (V_{CC} to GND)	I_{OUT} = 15A	43	48	54	V
T_{TSD}	Thermal shut-down temperature	V_{IN} = 3.25V	150	175	200	°C
T_{TR}	Thermal reset temperature		135			
T_{HYST}	Thermal hysteresis		7	15		

Table 11. Current sense ($9V < V_{CC} < 16V$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 30A; R_{SENSE} = 1.5kΩ; T_j = -40 to 150°C	9665	11370	13075	
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 8A; R_{SENSE} = 1.5kΩ; T_j = -40 to 150°C	9096	11370	13644	
dK_1 / K_1(1)	Analog sense current drift	I_{OUT} = 30A; R_{SENSE} = 1.5kΩ; T_j = -40 to 150°C	-8		+8	%
dK_2 / K_2(1)	Analog sense current drift	I_{OUT} > 8A; R_{SENSE} = 1.5kΩ; T_j = -40 to 150°C	-10		+10	
I_{SENSEO}	Analog sense leakage current	I_{OUT} = 0A; V_{SENSE} = 0V; T_j = -40 to 150°C	0		65	µA

1. Analog sense current drift is deviation of factor K for a given device over (-40°C to 150°C and $9V < V_{CC} < 16V$) with respect to its value measured at T_j = 25°C, V_{CC} = 13V.

Figure 4. Definition of the delay times measurement

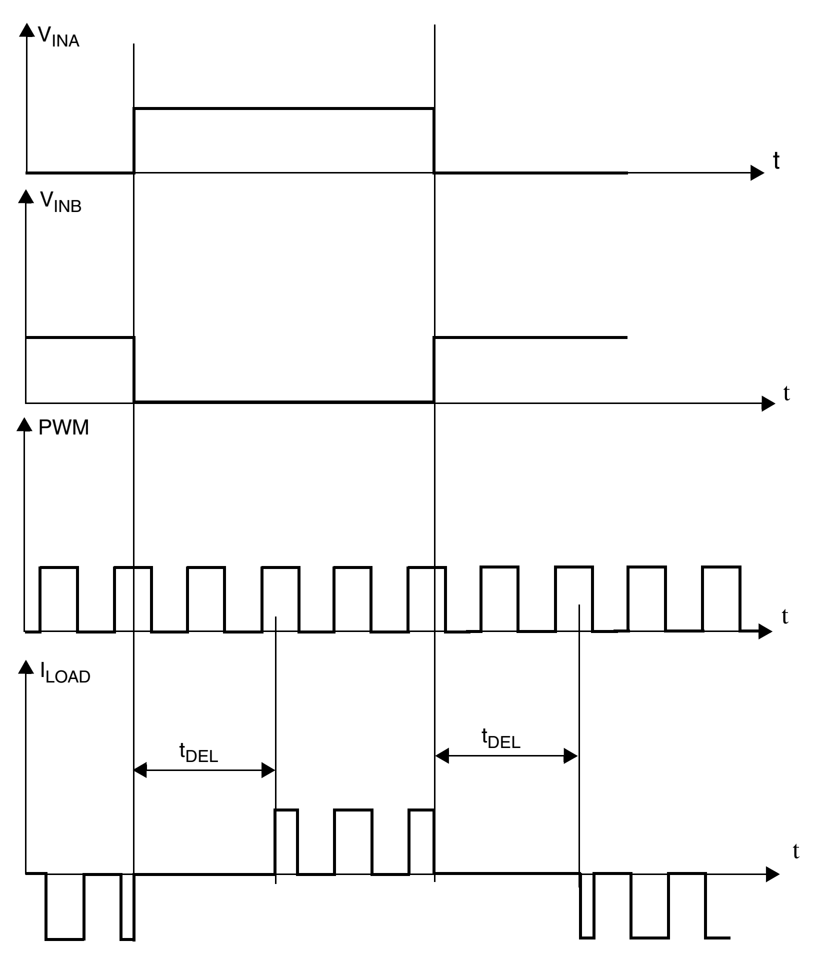


Figure 5. Definition of the low side switching times

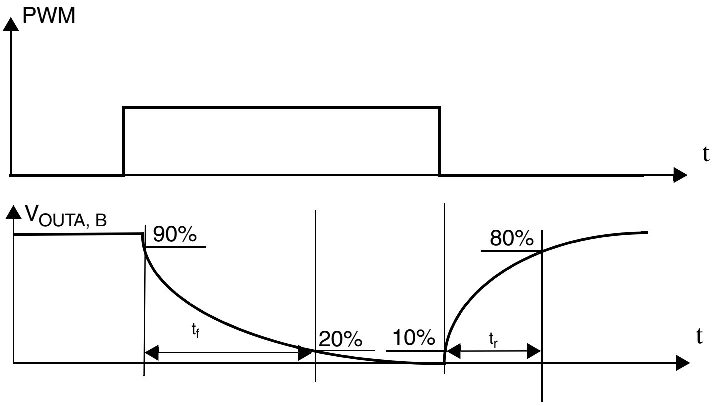


Figure 6. Definition of the high side switching times

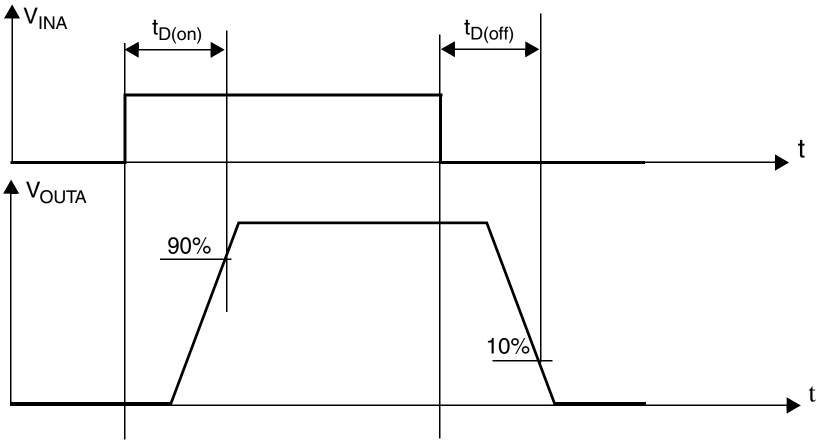


Figure 7. Definition of dynamic cross conduction current during a PWM operation

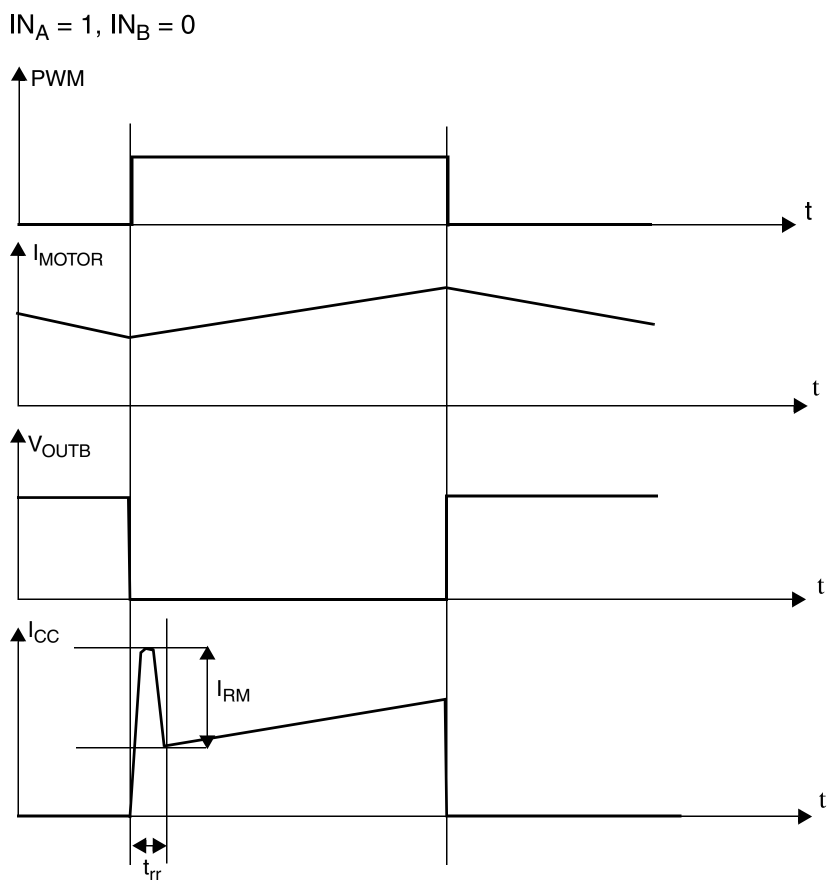


Table 12. Truth table in normal operating conditions

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS	Operating mode
1	1	1	1	H	H	High Imp.	Brake to V_{CC}
	0				L	$I_{SENSE} = I_{OUT}/K$	Clockwise (CW)
0	1			L	H		Counterclockwise (CCW)
	0				L	High Imp.	Brake to GND

Table 13. Truth table in fault conditions (detected on OUT_A)

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS
1	1	0	1	OPEN	H	High Imp.
	0				L	
0	1				H	I_{OUTB}/K
	0				L	High Imp.
X	X		0		OPEN	
	1		1		H	I_{OUTB}/K
	0				L	High Imp.
		Fault Information		Protection Action		

Note: Notice that saturation detection on the low side power MOSFET is possible only if the impedance of the short-circuit from the output to the battery is less than 100mΩ when the device is supplied with a battery voltage of 13.5V.

Table 14. Electrical transient requirements

ISO T/R - 7637/1 Test pulse	Test Level I	Test Level II	Test Level III	Test Level IV	Test levels delays and impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1µs, 50Ω
3b	+25V	+50V	+75V	+100V	
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R - 7637/1 test pulse	Test levels result I	Test levels result II	Test levels result III	Test levels result IV
1	C	C	C	C
2				
3a				
3b				
4				
5(1)		E	E	E

1. For load dump exceeding the above value a centralized suppressor must be adopted.

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.3 Electrical characteristics curves

Figure 8. On state supply current

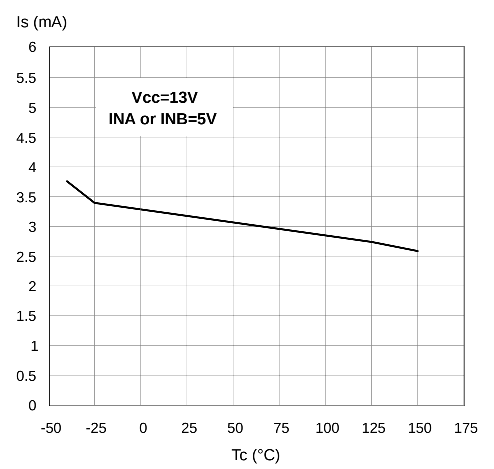


Figure 9. Off state supply current

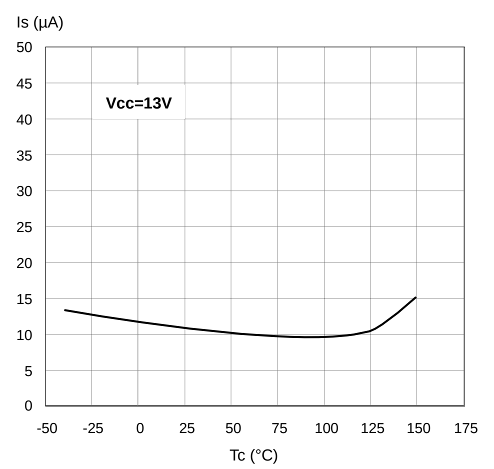


Figure 10. High level input current

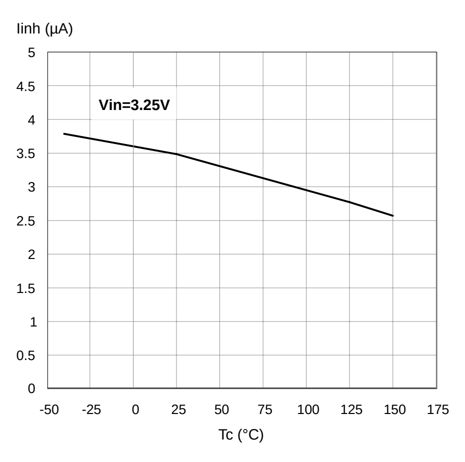


Figure 11. Input clamp voltage

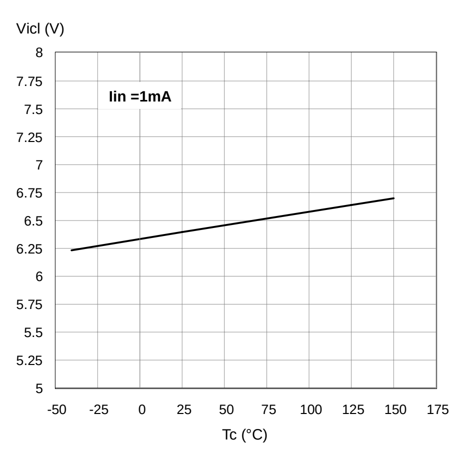


Figure 12. Input high level voltage

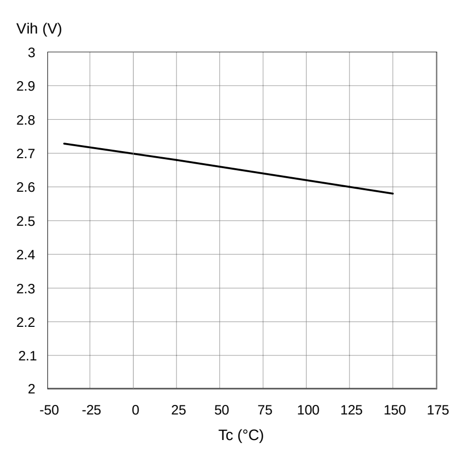


Figure 13. Input low level voltage

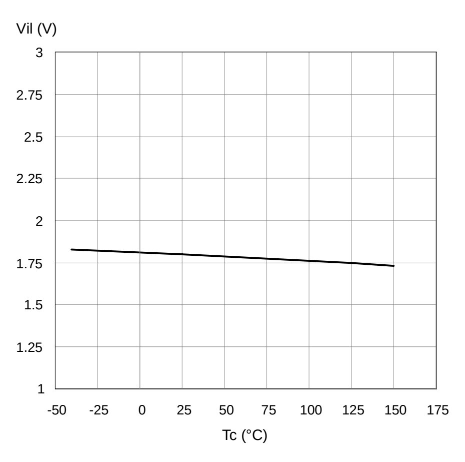


Figure 14. Input hysteresis voltage

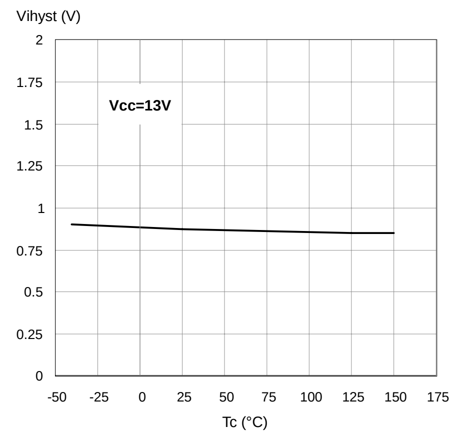


Figure 15. High level enable pin current

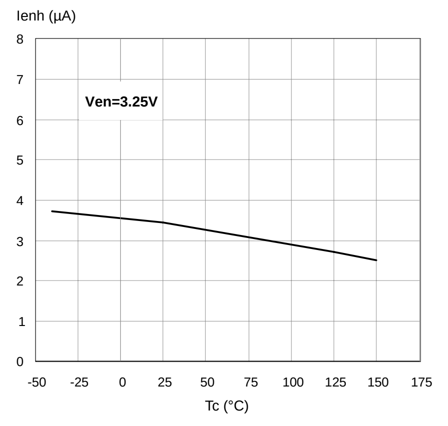


Figure 16. Delay time during change of operation mode

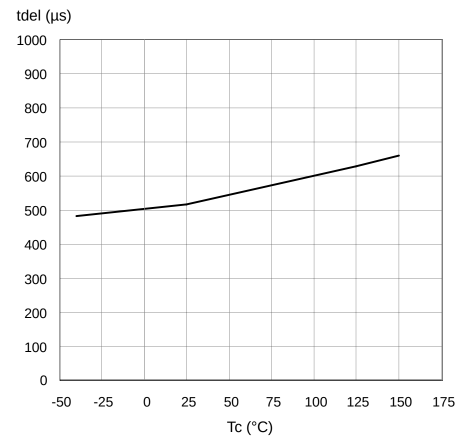


Figure 17. Enable clamp voltage

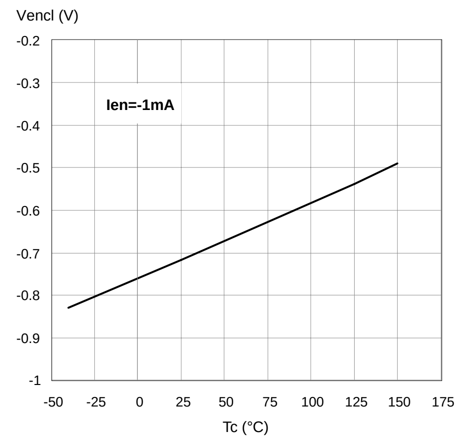


Figure 18. High level enable voltage

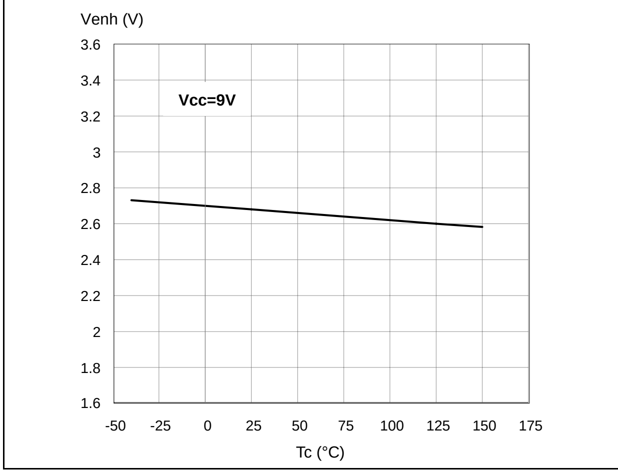


Figure 19. Low level enable voltage

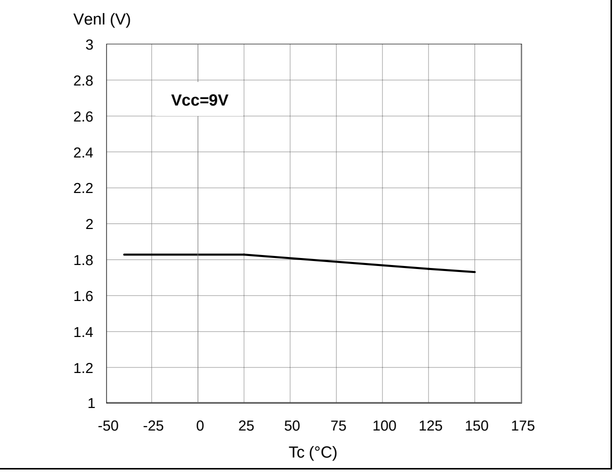


Figure 20. PWM high level voltage

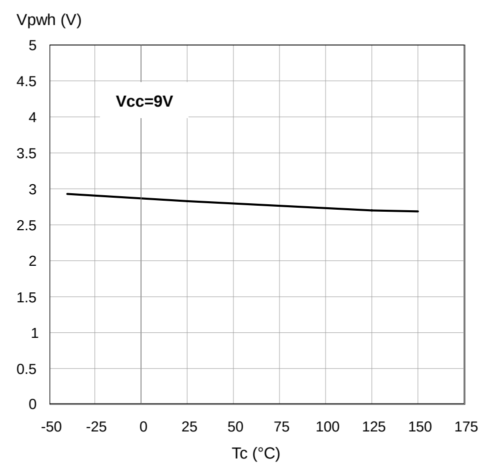


Figure 21. PWM low level voltage

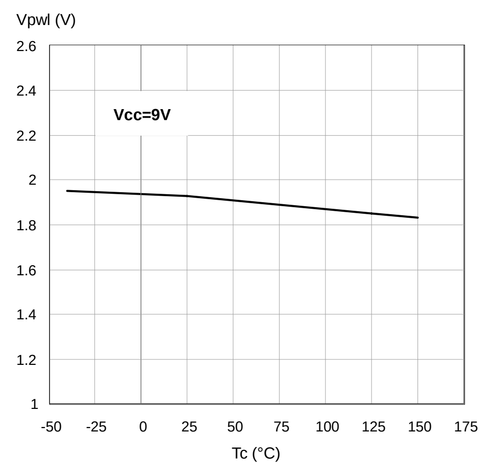


Figure 22. PWM high level current

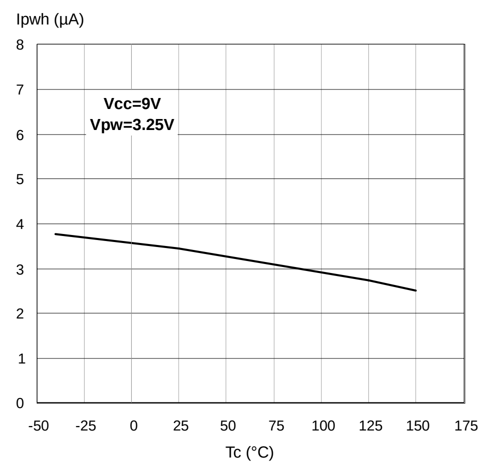


Figure 23. Overvoltage shutdown

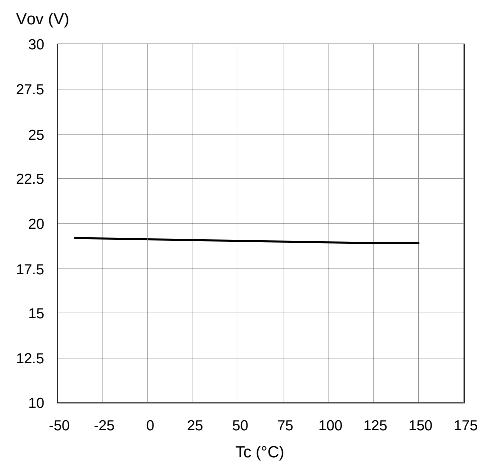


Figure 24. Undervoltage shutdown

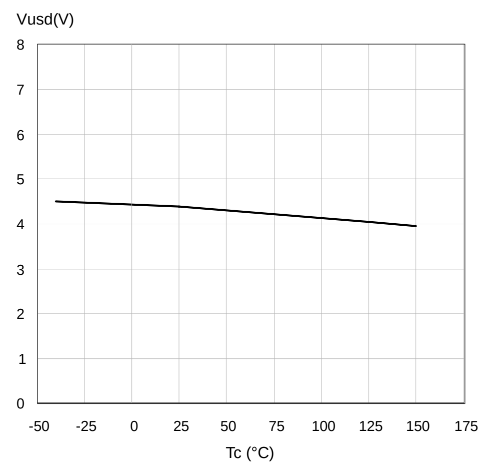


Figure 25. Current limitation

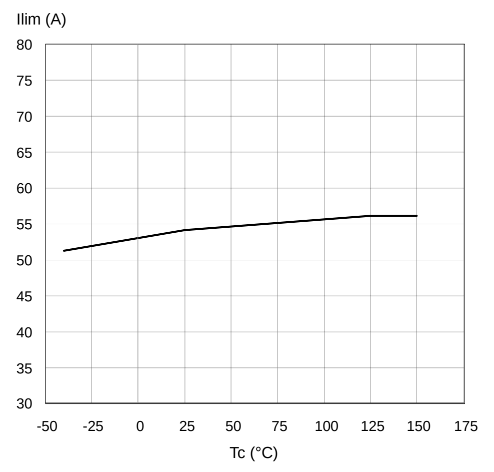


Figure 26. On state high side resistance vs T_{case}

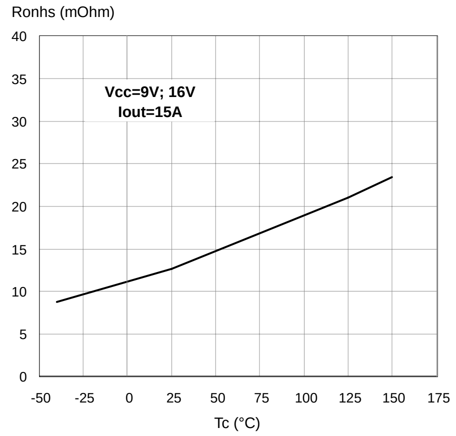


Figure 27. On state low side resistance vs T_{case}

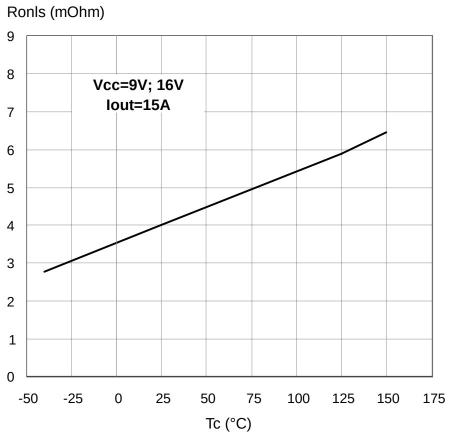


Figure 28. Turn-On delay time

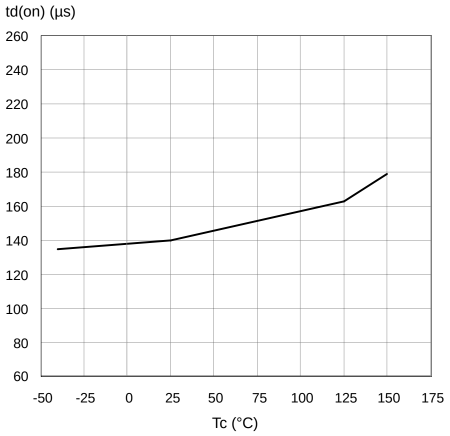


Figure 29. Turn-Off delay time

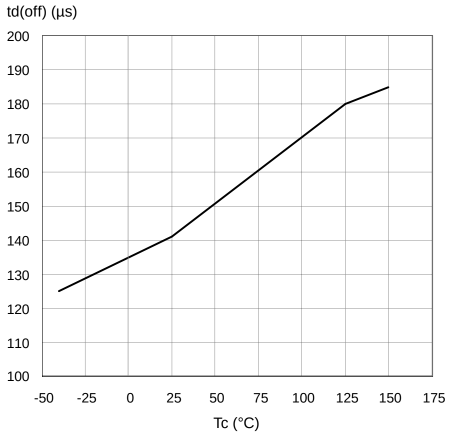


Figure 30. Output voltage rise time

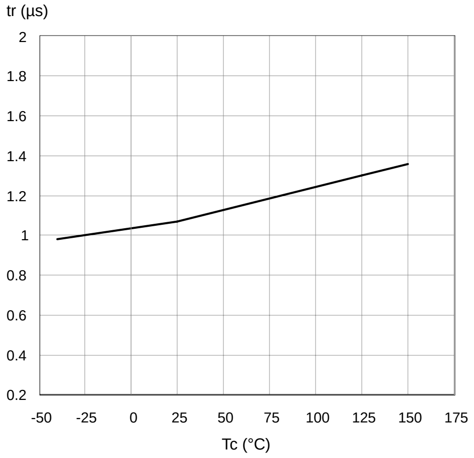
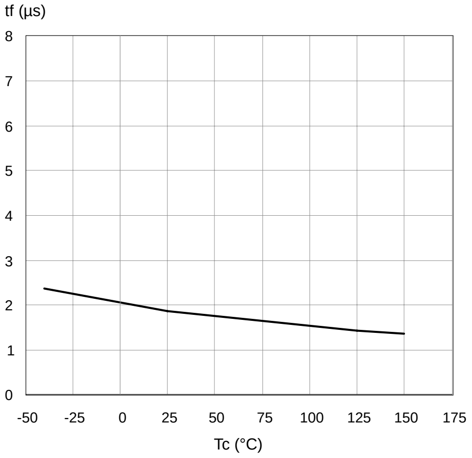


Figure 31. Output voltage fall time

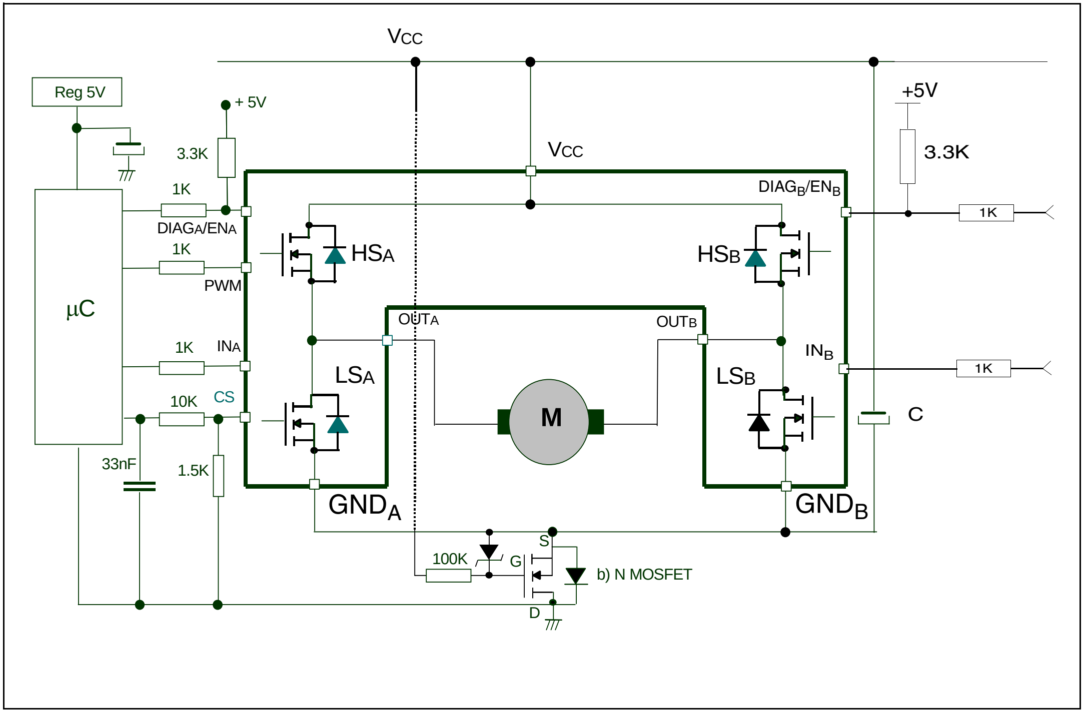


3 Application information

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

PWM pin usage: in all cases, a “0” on the PWM pin will turn off both LS_A and LS_B switches. When PWM rises back to “1”, LS_A or LS_B turn on again depending on the input pin state.

Figure 32. Typical application circuit for DC to 20 kHz PWM operation short circuit protection



Note: *The value of the blocking capacitor (C) depends on the application conditions and defines voltage and current ripple onto supply line at PWM operation. Stored energy of the motor inductance may fly back into the blocking capacitor, if the bridge driver goes into tri-state. This causes a hazardous overvoltage if the capacitor is not big enough. As basic orientation, 500µF per 10A load current is recommended.*

In case of a fault condition the $DIAG_X/EN_X$ pin is considered as an output pin by the device.The fault conditions are:

- overtemperature on one or both high sides
- short to battery condition on the output (saturation detection on the low side power MOSFET)

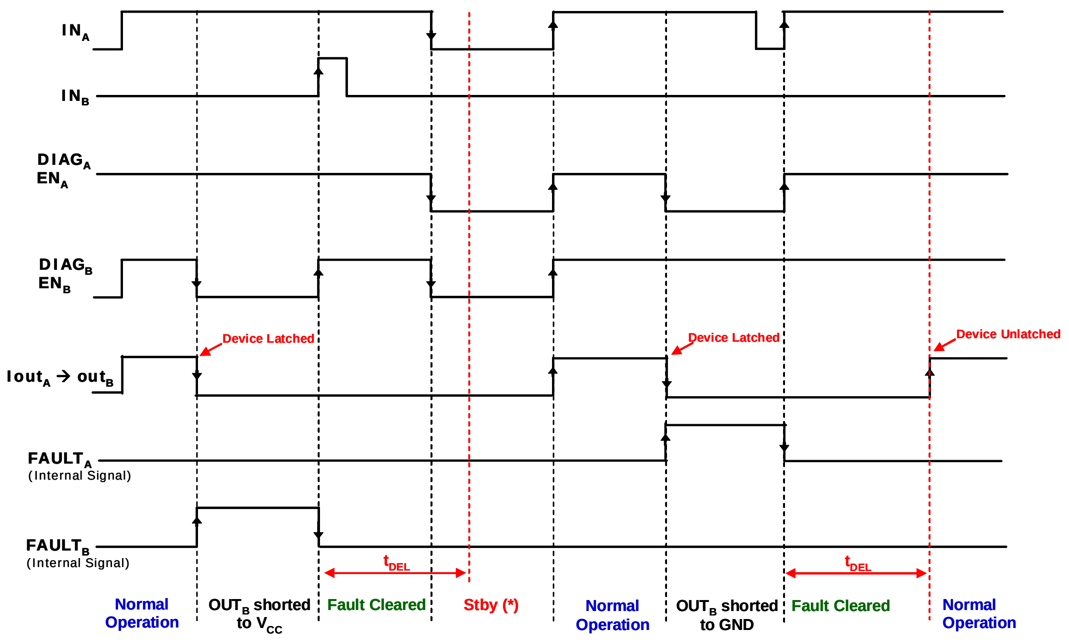
Possible origins of fault conditions may be:

- OUT_A is shorted to ground → overtemperature detection on high side A.
- OUT_A is shorted to V_{CC} → low side power MOSFET saturation detection.

When a fault condition is detected, the user can know which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn on the respective output (OUT_X) again, the input signal must rise from low to high level.

Figure 33. Behavior in fault condition (How a fault can be cleared)



Note: *In case of the fault condition is not removed, the procedure for unlatching and sending the device in Stby mode is:*

- Clear the fault in the device (toggle : INA if ENA=0 or INB if ENB=0)

- Pull low all inputs, PWM and Diag/EN pins within tDEL.

If the Diag/En pins are already low, PWM=0, the fault can be cleared simply toggling the input. The device will enter in stby mode as soon as the fault is cleared.

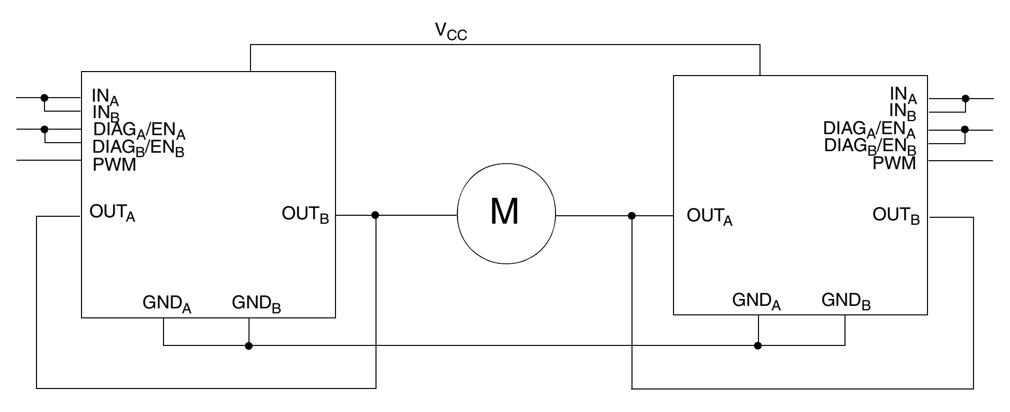
3.1 Reverse battery protection

Three possible solutions can be considered:

1. a Schottky diode D connected to V_{CC} pin
2. an N-channel MOSFET connected to the GND pin (see *Figure 32: Typical application circuit for DC to 20 kHz PWM operation short circuit protection on page 20*)
3. a P-channel MOSFET connected to the V_{CC} pin

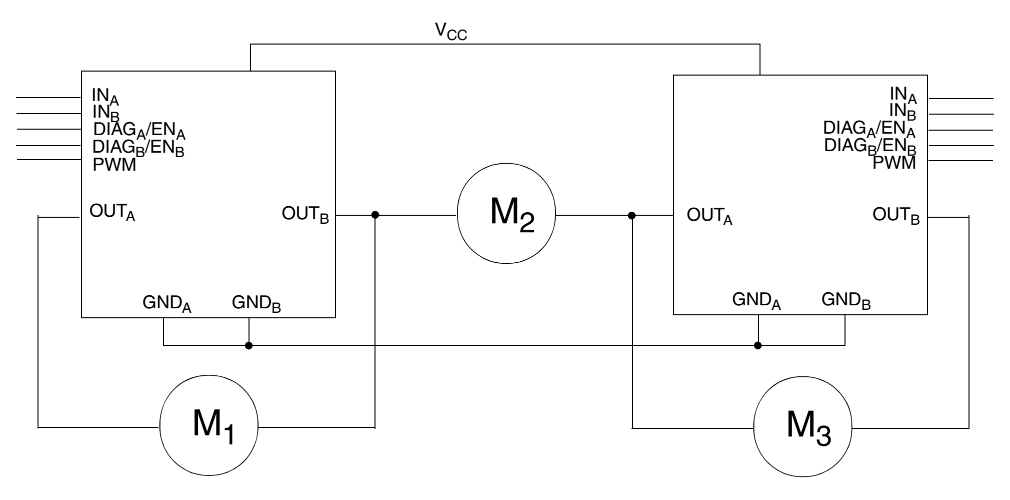
The device sustains no more than -30A in reverse battery conditions because of the two body diodes of the power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH2SP30-E are pulled down to the V_{CC} line (approximately -1.5V). A series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I_{Rmax} is the maximum target reverse current through µC I/Os, the series resistor is:

Figure 34. Half-bridge configuration



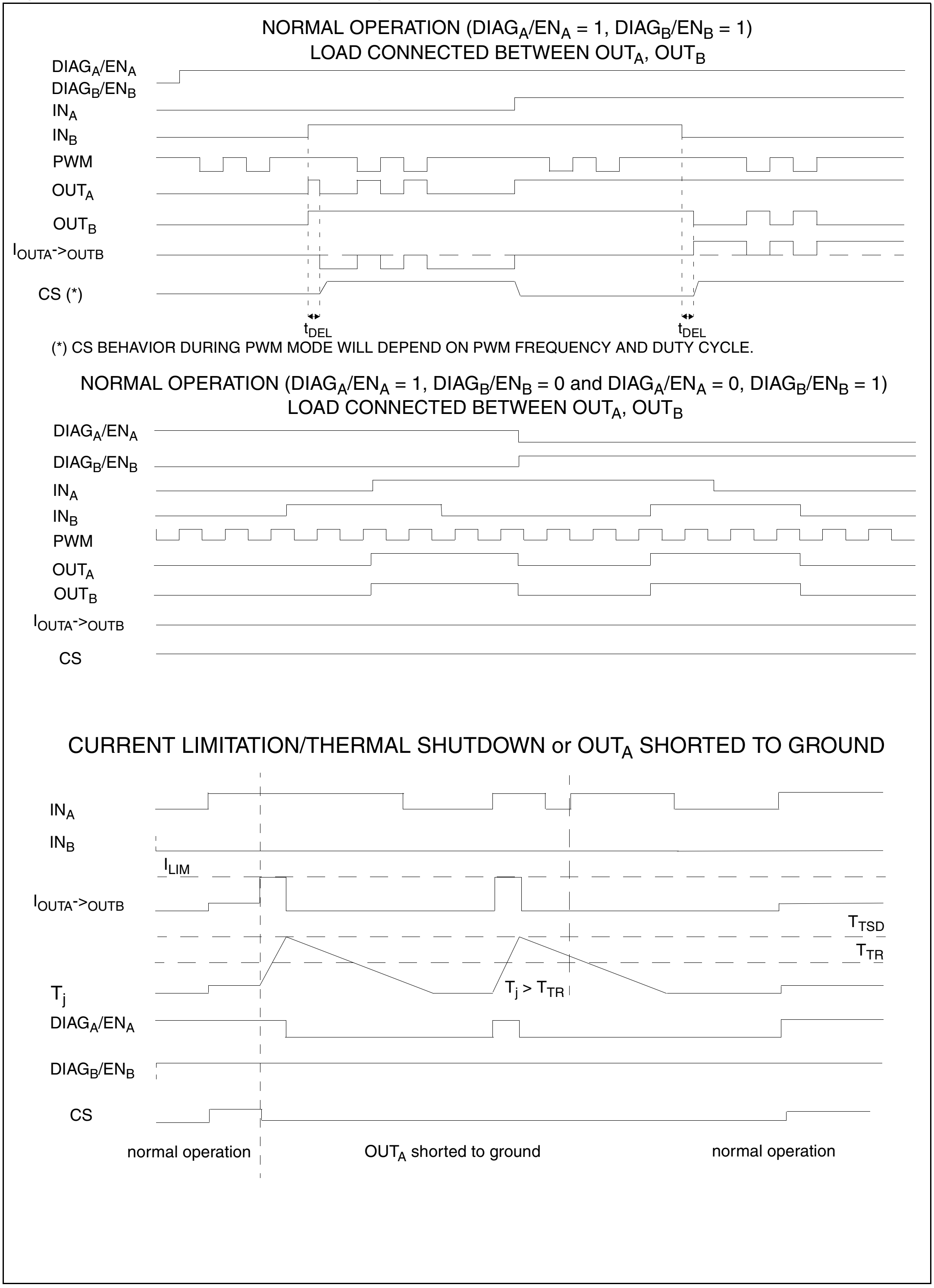
Note: *The VNH2SP30-E can be used as a high power half-bridge driver achieving an On resistance per leg of 9.5mΩ.*

Figure 35. Multi-motors configuration



Note: *The VNH2SP30-E can easily be designed in multi-motors driving applications such as seat positioning systems where only one motor must be driven at a time. $DIAG_X/EN_X$ pins allow to put unused half-bridges in high impedance.*

Figure 36. Waveforms in full bridge operation



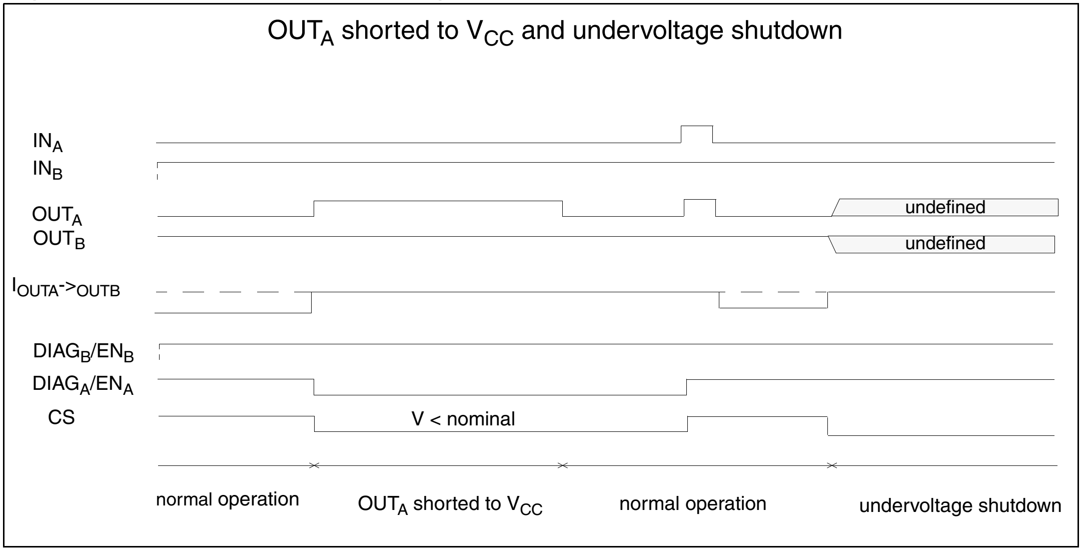
NORMAL OPERATION (DIAG$_A$/EN$_A$ = 1, DIAG$_B$/EN$_B$ = 1)
LOAD CONNECTED BETWEEN OUT$_A$, OUT$_B$

(*) CS BEHAVIOR DURING PWM MODE WILL DEPEND ON PWM FREQUENCY AND DUTY CYCLE.

NORMAL OPERATION (DIAG$_A$/EN$_A$ = 1, DIAG$_B$/EN$_B$ = 0 and DIAG$_A$/EN$_A$ = 0, DIAG$_B$/EN$_B$ = 1)
LOAD CONNECTED BETWEEN OUT$_A$, OUT$_B$

CURRENT LIMITATION/THERMAL SHUTDOWN or OUT$_A$ SHORTED TO GROUND

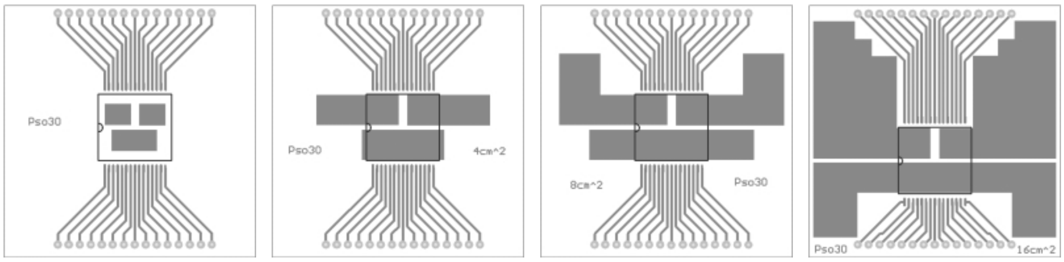
Figure 37. Waveforms in full bridge operation (continued)



4 Package and PCB thermal data

4.1 PowerSSO-30 thermal data

Figure 38. MultiPowerSO-30™ PC board



Note: *Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm. Cu thickness = 35µm, Copper areas: from minimum pad layout to 16cm^2).*

Figure 39. Chipset configuration

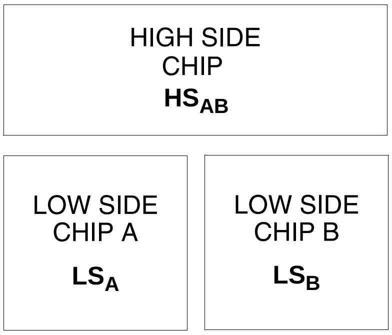
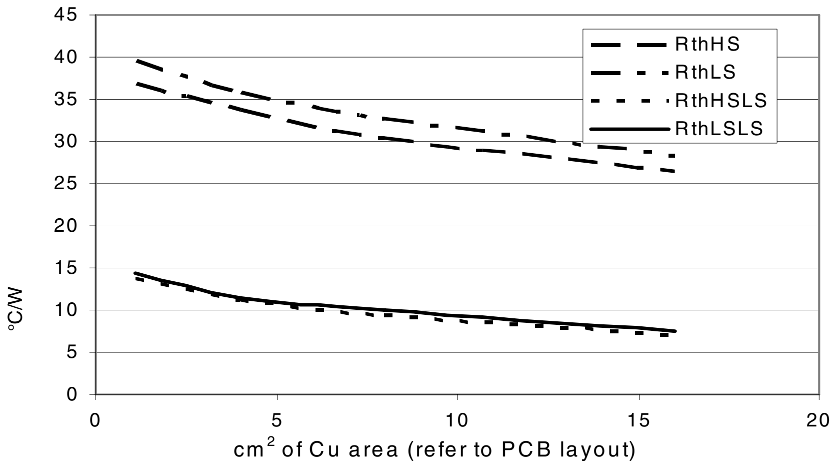


Figure 40. Auto and mutual $R_{thj-amb}$ vs PCB copper area in open box free air condition



4.1.1 Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Table 15. Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

HS_A	HS_B	LS_A	LS_B	T_{jHSAB}	T_{jLSA}	T_{jLSB}
ON	OFF	OFF	ON	$P_{dHSA} \times R_{thHS} + P_{dLSB} \times R_{thHSLS} + T_{amb}$	$P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLSLS} + T_{amb}$	$P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLS} + T_{amb}$
OFF	ON	ON	OFF	$P_{dHSB} \times R_{thHS} + P_{dLSA} \times R_{thHSLS} + T_{amb}$	$P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLS} + T_{amb}$	$P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLSLS} + T_{amb}$

4.1.2 Thermal resistances definition (values according to the PCB heatsink area)

R_{thHS} = R_{thHSA} = R_{thHSB} = High Side Chip Thermal Resistance Junction to Ambient (HS_A or HS_B in ON state)

R_{thLS} = R_{thLSA} = R_{thLSB} = Low Side Chip Thermal Resistance Junction to Ambient

R_{thHSLS} = $R_{thHSALSB}$ = $R_{thHSBLSA}$ = Mutual Thermal Resistance Junction to Ambient between High Side and Low Side Chips

R_{thLSLS} = $R_{thLSALSB}$ = Mutual Thermal Resistance Junction to Ambient between Low Side Chips

4.1.3 Thermal calculation in transient mode[a]

$T_{jHSAB} = Z_{thHS} \times P_{dHSAB} + Z_{thHSLS} \times (P_{dLSA} + P_{dLSB}) + T_{amb}$

$T_{jLSA} = Z_{thHSLS} \times P_{dHSAB} + Z_{thLS} \times P_{dLSA} + Z_{thLSLS} \times P_{dLSB} + T_{amb}$

$T_{jLSB} = Z_{thHSLS} \times P_{dHSAB} + Z_{thLSLS} \times P_{dLSA} + Z_{thLS} \times P_{dLSB} + T_{amb}$

4.1.4 Single pulse thermal impedance definition (values according to the PCB heatsink area)

Z_{thHS} = High Side Chip Thermal Impedance Junction to Ambient

Z_{thLS} = Z_{thLSA} = Z_{thLSB} = Low Side Chip Thermal Impedance Junction to Ambient

Z_{thHSLS} = $Z_{thHSABLSA}$ = $Z_{thHSABLSB}$ = Mutual Thermal Impedance Junction to Ambient between High Side and Low Side Chips

Z_{thLSLS} = $Z_{thLSALSB}$ = Mutual Thermal Impedance Junction to Ambient between Low Side Chips

---

[a] Calculation is valid in any dynamic operating condition. P_d values set by user.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 41. MultiPowerSO-30 HSD thermal impedance junction ambient single pulse

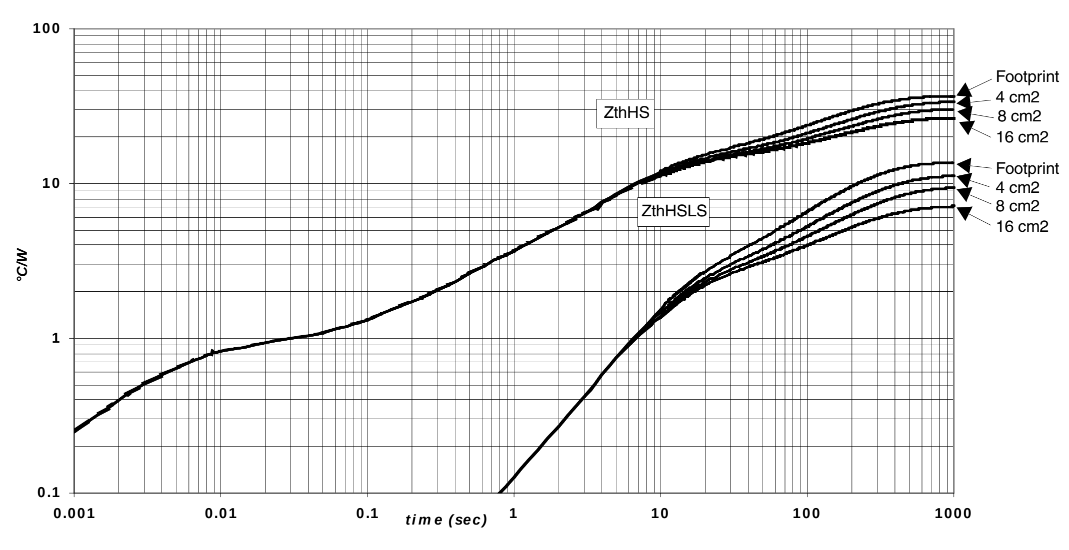


Figure 42. MultiPowerSO-30 LSD thermal impedance junction ambient single pulse

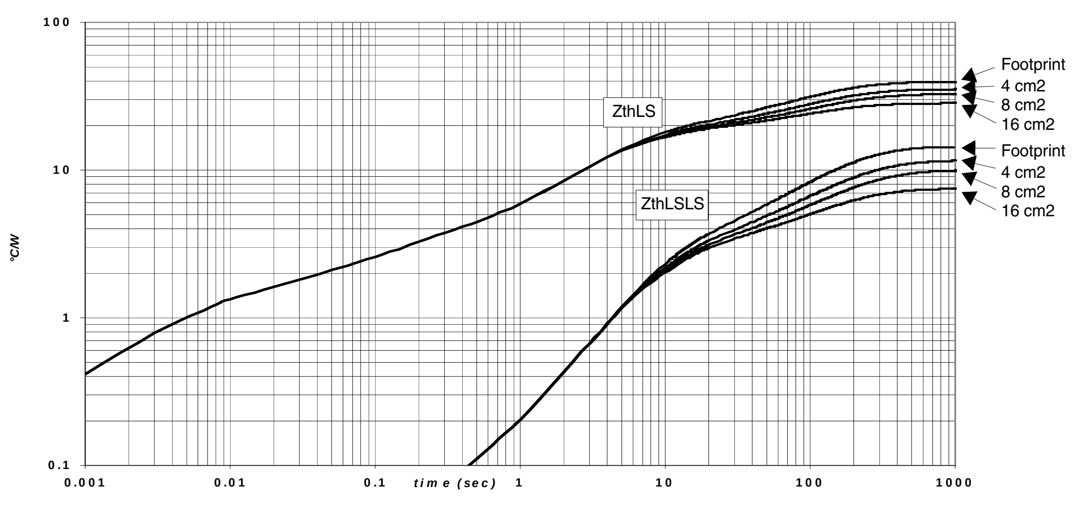


Figure 43. Thermal fitting model of an H-bridge in MultiPowerSO-30

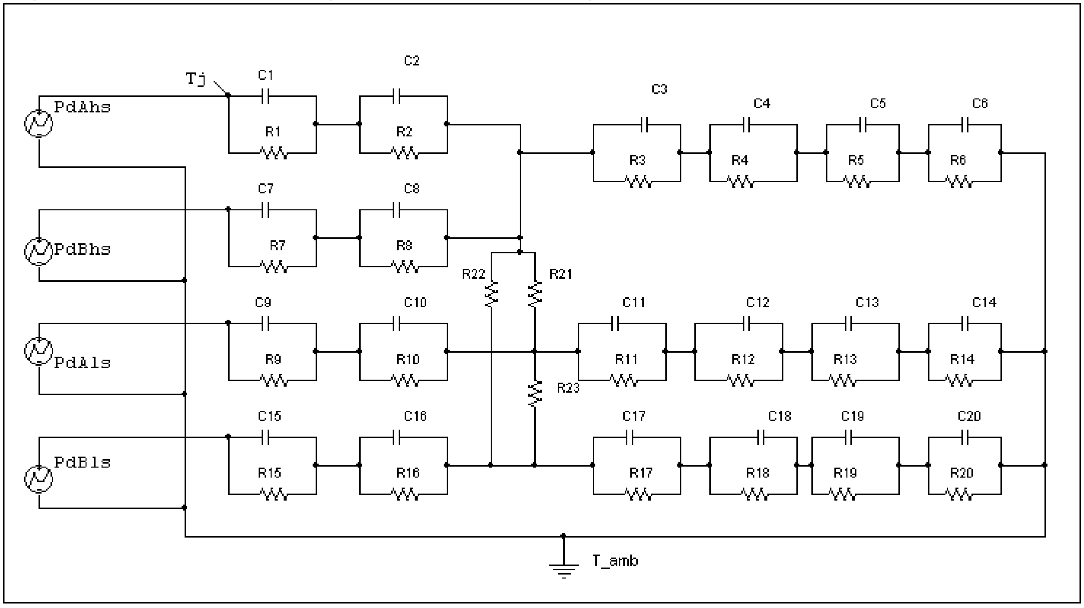


Table 16. Thermal parameters[1]

Area/island (cm^2)	Footprint	4	8	16
R1 = R7 (°C/W)	0.05			
R2 = R8 (°C/W)	0.3			
R3 (°C/W)	0.5			
R4 (°C/W)	1.3			
R5 (°C/W)	14			
R6 (°C/W)	44.7	39.1	31.6	23.7
R9 = R15 (°C/W)	0.2			
R10 = R16 (°C/W)	0.4			
R11 = R17 (°C/W)	0.8			
R12 = R18 (°C/W)	1.5			
R13 = R19 (°C/W)	20			
R14 = R20 (°C/W)	46.9	36.1	30.4	20.8
R21 = R22 = R23 (°C/W)	115			
C1 = C7 (W.s/°C)	0.005			
C2 = C8 (W.s/°C)	0.008			
C3 = C11 = C17 (W.s/°C)	0.01			
C4 = C13 = C19 (W.s/°C)	0.3			
C5 (W.s/°C)	0.6			
C6 (W.s/°C)	5	7	9	11
C9 = C15 (W.s/°C)	0.003			
C10 = C16 (W.s/°C)	0.006			
C12 = C18 (W.s/°C)	0.075			
C14 = C20 (W.s/°C)	2.5	3.5	4.5	5.5

1. The blank space means that the value is the same as the previous one.

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

5.2 MultiPowerSO-30 package mechanical data

Figure 44. MultiPowerSO-30 package outline

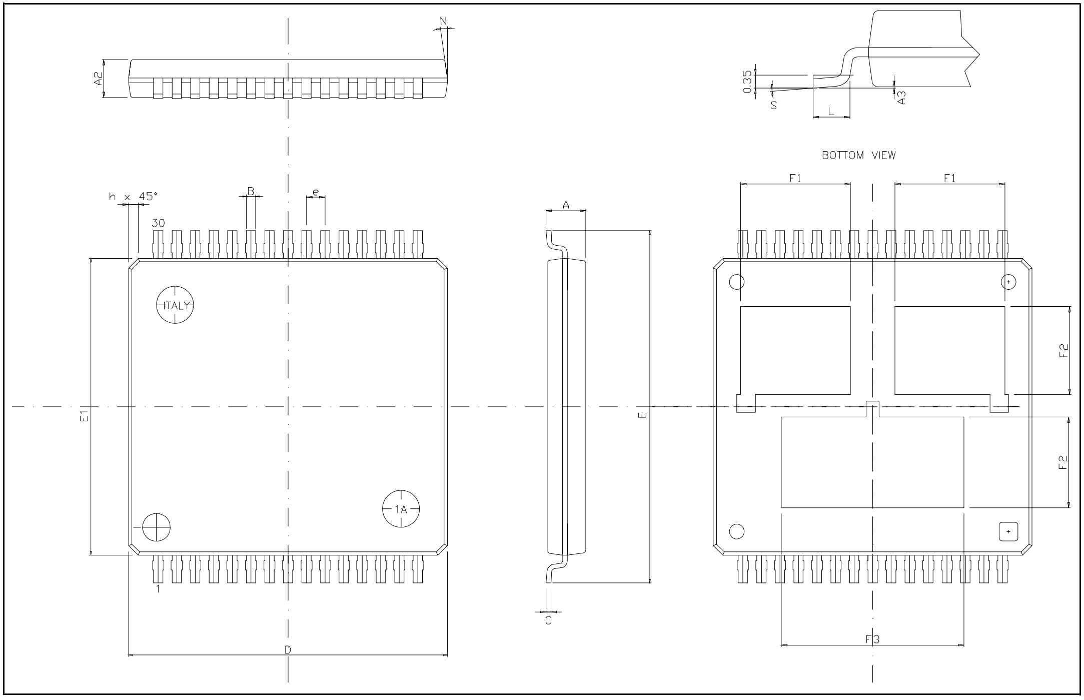
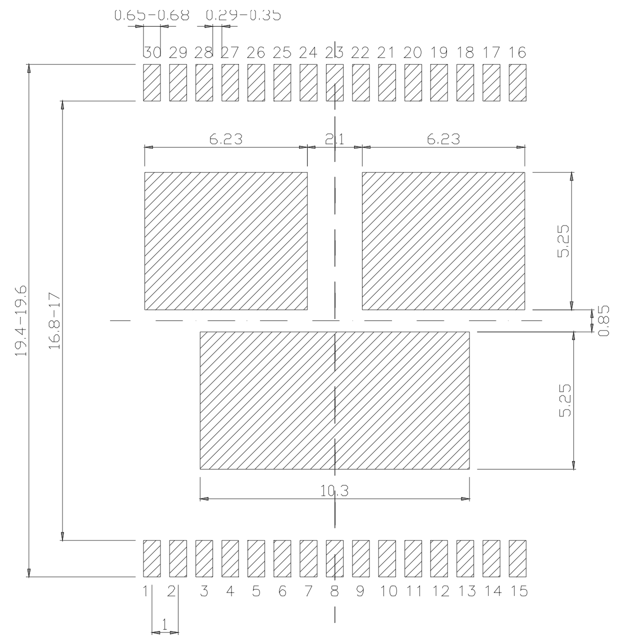


Table 17. MultiPowerSO-30 mechanical data

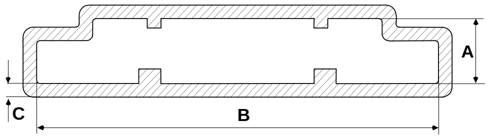
Symbol	Millimeters		
	Min	Typ	Max
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1
e		1	
F1	5.55		6.05
F2	4.6		5.1
F3	9.6		10.1
L	0.8		1.15
N			10deg
S	0deg		7deg

Figure 45. MultiPowerSO-30 suggested pad layout



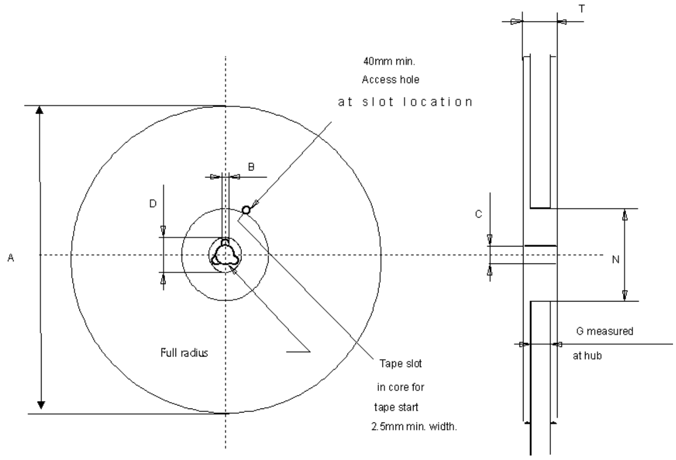
5.3 Packing information

Note: The devices can be packed in tube or tape and reel shipments (see the Device summary on page 1 for packaging quantities).



Dimension	mm
Base Q.ty	29
Bulk Q.ty	435
Tube length (± 0.5)	532
A	3.82
B	23.6
C (± 0.13)	0.8

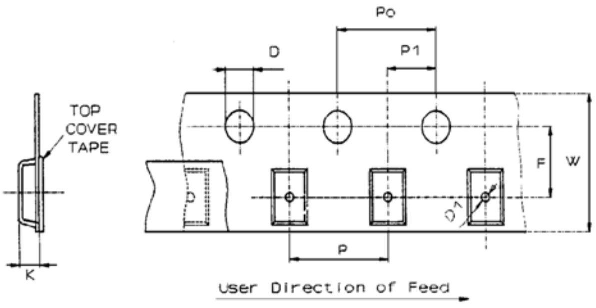
Figure 46. MultiPowerSO-30 tube shipment (no suffix)



Reel dimensions

SO-28 tube shipment (no suffix)

Dimension	mm
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
D (min)	20.2
G (+ 2 / -0)	32
N (min)	100
T (max)	38.4



Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Description	Dimension	mm
Tape width	W	32
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	2
Hole Position	F (± 0.1)	14.2
Compartment Depth	K (max)	2.2

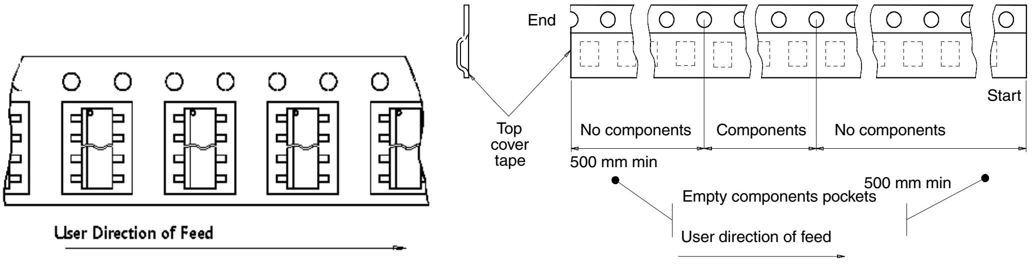


Figure 47. MultiPowerSO-30 tape and reel shipment (suffix "TR")

6 Revision history

Table 18. Document revision history

Date	Revision	Description of changes
Sep-2004	1	First issue
Dec- 2004	2	Inserted $t_{off(min)}$ test condition modification and note Modified I_{RM} figure number
Feb-2005	3	Minor changes
Apr-2005	4	Public release
01-Sep-2006	5	Document converted into new ST corporate template. Added table of contents, list of tables and list of figures Removed figure number from package outline *on page 1* Changed *Features on page 1* to add ECOPACK® package Added *Section 1: Block diagram and pin description on page 5* Added *Section 2.2: Electrical characteristics on page 9* Added “low” and “high” to parameters for I_{INL} and I_{INH} in *Table 7 on page 9* Inserted note in *Figure 32 on page 20* Added vertical limitation line to left side arrow of $t_{D(off)}$ to *Figure 7 on page 13* Added *Section 4.1: PowerSSO-30 thermal data on page 25* Added *Section 5: Package and packing information on page 29* Added *Section 5.3: Packing information on page 31* Updated disclaimer (last page) to include a mention about the use of ST products in automotive applications
15-May-2007	6	Document reformatted and converted into new ST template.
06-Feb-2008	7	Corrected Heat Slug numbers in *Table 3: Pin definitions and functions*.
02-Oct-2008	8	Added new infomation in *Table 6: Power section* Added *Figure 33: Behavior in fault condition (How a fault can be cleared)*

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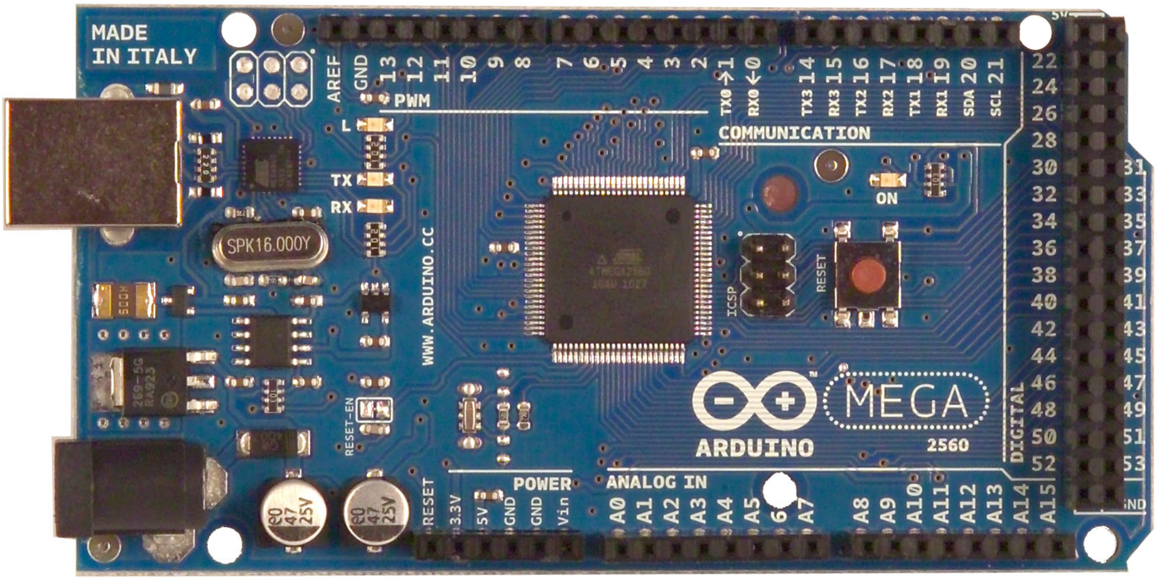
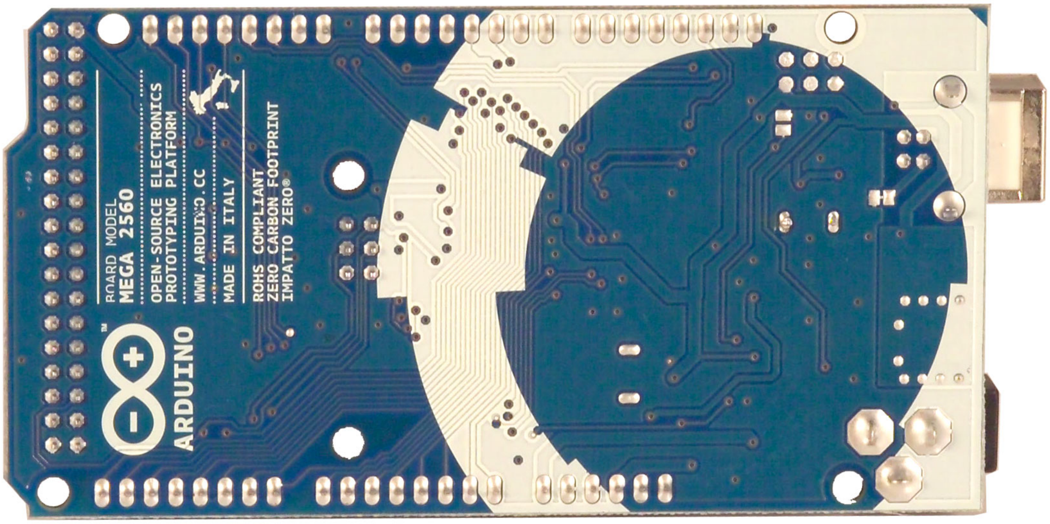
ARDUINO

Arduino Mega 2560 Datasheet





Overview

The Arduino Mega 2560 is a microcontroller board based on the ATmega2560 (datasheet). It has 54 digital input/output pins (of which 14 can be used as PWM outputs), 16 analog inputs, 4 UARTs (hardware serial ports), a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with a AC-to-DC adapter or battery to get started. The Mega is compatible with most shields designed for the Arduino Duemilanove or Diecimila.

Schematic & Reference Design

EAGLE files: arduino-mega2560-reference-design.zip

Schematic: arduino-mega2560-schematic.pdf

Summary

Microcontroller	ATmega2560
Operating Voltage	5V
Input Voltage (recommended)	7-12V
Input Voltage (limits)	6-20V
Digital I/O Pins	54 (of which 14 provide PWM output)
Analog Input Pins	16
DC Current per I/O Pin	40 mA
DC Current for 3.3V Pin	50 mA
Flash Memory	256 KB of which 8 KB used by bootloader
SRAM	8 KB
EEPROM	4 KB
Clock Speed	16 MHz

Power

The Arduino Mega can be powered via the USB connection or with an external power supply. The power source is selected automatically.

External (non-USB) power can come either from an AC-to-DC adapter (wall-wart) or battery. The adapter can be connected by plugging a 2.1mm center-positive plug into the board's power jack. Leads from a battery can be inserted in the Gnd and Vin pin headers of the POWER connector.

The board can operate on an external supply of 6 to 20 volts. If supplied with less than 7V, however, the 5V pin may supply less than five volts and the board may be unstable. If using more than 12V, the voltage regulator may overheat and damage the board. The recommended range is 7 to 12 volts.

The Mega2560 differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega8U2 programmed as a USB-to-serial converter.

The power pins are as follows:

- **VIN.** The input voltage to the Arduino board when it's using an external power source (as opposed to 5 volts from the USB connection or other regulated power source). You can supply voltage through this pin, or, if supplying voltage via the power jack, access it through this pin.
- **5V.** The regulated power supply used to power the microcontroller and other components on the board. This can come either from VIN via an on-board regulator, or be supplied by USB or another regulated 5V supply.
- **3V3.** A 3.3 volt supply generated by the on-board regulator. Maximum current draw is 50 mA.
- **GND.** Ground pins.

Memory

The ATmega2560 has 256 KB of flash memory for storing code (of which 8 KB is used for the bootloader), 8 KB of SRAM and 4 KB of EEPROM (which can be read and written with the EEPROM library).

Input and Output

Each of the 54 digital pins on the Mega can be used as an input or output, using pinMode() , digitalWrite(), and digitalRead() functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

- **Serial: 0 (RX) and 1 (TX); Serial 1: 19 (RX) and 18 (TX); Serial 2: 17 (RX) and 16 (TX); Serial 3: 15 (RX) and 14 (TX).** Used to receive (RX) and transmit (TX) TTL serial data. Pins 0 and 1 are also connected to the corresponding pins of the ATmega8U2 USB-to-TTL Serial chip.
- **External Interrupts: 2 (interrupt 0), 3 (interrupt 1), 18 (interrupt 5), 19 (interrupt 4), 20 (interrupt 3), and 21 (interrupt 2).** These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value. See the attachInterrupt() function for details.
- **PWM: 0 to 13.** Provide 8-bit PWM output with the analogWrite() function.
- **SPI: 50 (MISO), 51 (MOSI), 52 (SCK), 53 (SS).** These pins support SPI communication using the SPI library. The SPI pins are also broken out on the ICSP header, which is physically compatible with the Uno, Duemilanove and Diecimila.
- **LED: 13.** There is a built-in LED connected to digital pin 13. When the pin is HIGH

value, the LED is on, when the pin is LOW, it's off.

- **I2C: 20 (SDA) and 21 (SCL).** Support I2C (TWI) communication using the Wire library (documentation on the Wiring website). Note that these pins are not in the same location as the I2C pins on the Duemilanove or Diecimila.

The Mega2560 has 16 analog inputs, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the AREF pin and analogReference() function.

There are a couple of other pins on the board:

- **AREF.** Reference voltage for the analog inputs. Used with analogReference().
- **Reset.** Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

Communication

The Arduino Mega2560 has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega2560 provides four hardware UARTs for TTL (5V) serial communication. An ATmega8U2 on the board channels one of these over USB and provides a virtual com port to software on the computer (Windows machines will need a .inf file, but OSX and Linux machines will recognize the board as a COM port automatically. The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the board. The RX and TX LEDs on the board will flash when data is being transmitted via the ATmega8U2 chip and USB connection to the computer (but not for serial communication on pins 0 and 1).
A SoftwareSerial library allows for serial communication on any of the Mega2560's digital pins.
The ATmega2560 also supports I2C (TWI) and SPI communication. The Arduino software includes a Wire library to simplify use of the I2C bus; see the documentation on the Wiring website for details. For SPI communication, use the SPI library.

Programming

The Arduino Mega can be programmed with the Arduino software (download). For details, see the reference and tutorials.
The ATmega2560 on the Arduino Mega comes preburned with a bootloader that allows you to upload new code to it without the use of an external hardware programmer. It

communicates using the original STK500 protocol (reference, C header files).
You can also bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header; see these instructions for details.

Automatic (Software) Reset

Rather then requiring a physical press of the reset button before an upload, the Arduino Mega2560 is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the ATmega8U2 is connected to the reset line of the ATmega2560 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload.
This setup has other implications. When the Mega2560 is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Mega2560. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened.
If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.
The Mega2560 contains a trace that can be cut to disable the auto-reset. The pads on either side of the trace can be soldered together to re-enable it. It's labeled "RESET-EN". You may also be able to disable the auto-reset by connecting a 110 ohm resistor from 5V to the reset line; see this forum thread for details.

USB Overcurrent Protection

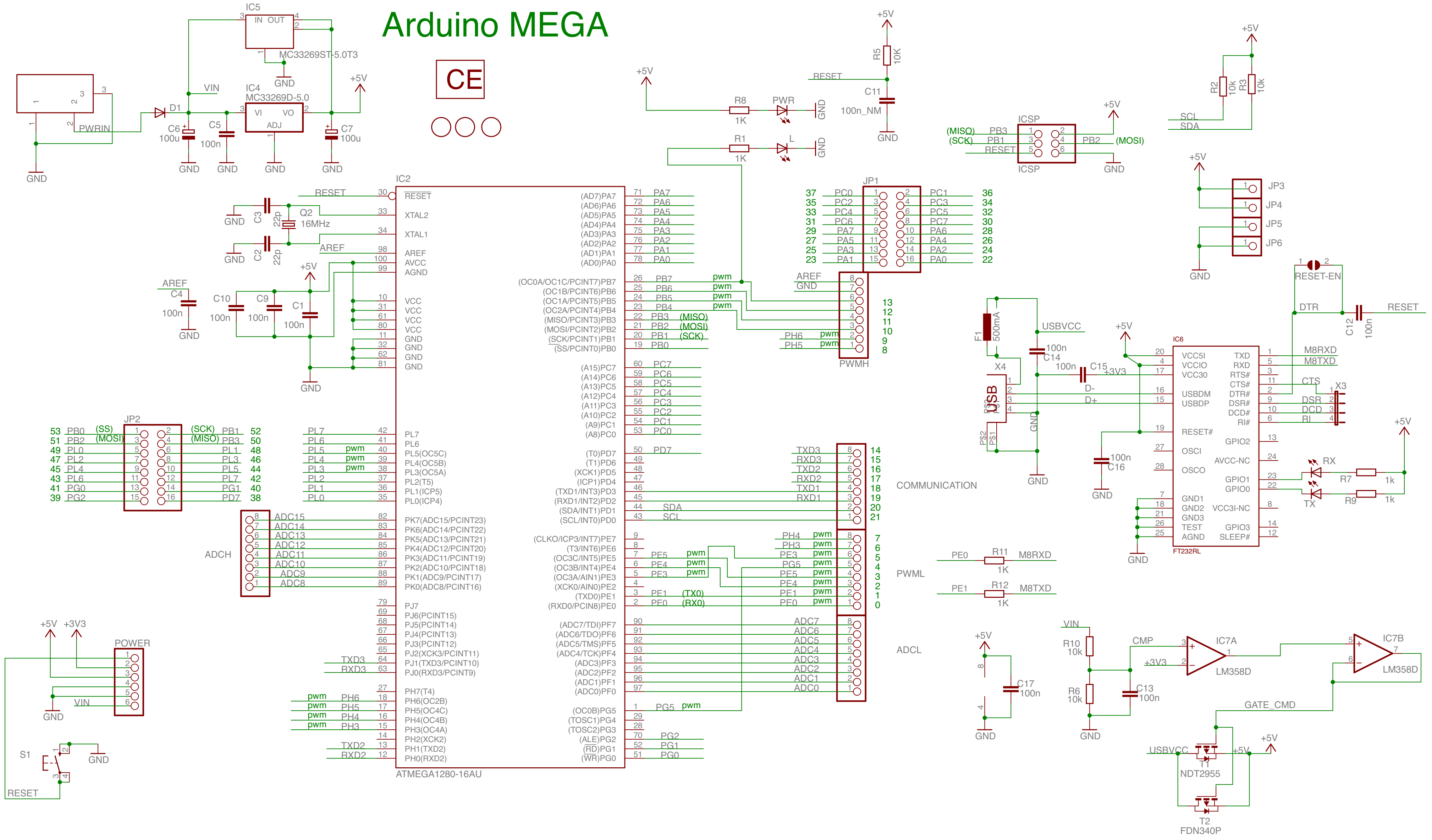
The Arduino Mega2560 has a resettable polyfuse that protects your computer's USB ports from shorts and overcurrent. Although most computers provide their own internal protection, the fuse provides an extra layer of protection. If more than 500 mA is applied to the USB port, the fuse will automatically break the connection until the short or overload is removed.

Physical Characteristics and Shield Compatibility

The maximum length and width of the Mega2560 PCB are 4 and 2.1 inches respectively, with the USB connector and power jack extending beyond the former dimension. Three screw holes allow the board to be attached to a surface or case. Note that the distance between digital pins 7 and 8 is 160 mil (0.16"), not an even multiple of the 100 mil spacing of the other pins.

The Mega2560 is designed to be compatible with most shields designed for the Uno, Diecimila or Duemilanove. Digital pins 0 to 13 (and the adjacent AREF and GND pins), analog inputs 0 to 5, the power header, and ICSP header are all in equivalent locations. Further the main UART (serial port) is located on the same pins (0 and 1), as are external interrupts 0 and 1 (pins 2 and 3 respectively). SPI is available through the ICSP header on both the Mega2560 and Duemilanove / Diecimila. *Please note that I$_2$C is not located on the same pins on the Mega (20 and 21) as the Duemilanove / Diecimila (analog inputs 4 and 5).*

Arduino MEGA



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MFRC522

Contactless Reader IC

Rev. 3.2 — 22 May 2007
112132

Product data sheet
PUBLIC INFORMATION

1. Introduction

This document describes the functionality of the contactless reader/writer MFRC522. It includes the functional and electrical specifications.

2. General description

The MFRC522 is a highly integrated reader/writer for contactless communication at 13.56 MHz. The MFRC522 reader supports ISO 14443A / MIFARE® mode.

The MFRC522's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A/MIFARE® cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443A/MIFARE® compatible cards and transponders. The digital part handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).The MFRC522 supports MIFARE®Classic (e.g. MIFARE® Standard) products. The MFRC522 supports contactless communication using MIFARE® higher transfer speeds up to 848 kbit/s in both directions.

Various host interfaces are implemented:

- SPI interface
- serial UART (similar to RS232 with voltage levels according pad voltage supply)
- I^{2}C interface.

3. Features

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers to connect an antenna with minimum number of external components
- Supports ISO/IEC 14443A / MIFARE®
- Typical operating distance in Reader/Writer mode for communication to a ISO/IEC 14443A / MIFARE® up to 50 mm depending on the antenna size and tuning
- Supports MIFARE® Classic encryption in Reader/Writer mode
- Supports ISO/IEC 14443A higher transfer speed communication up to 848 kbit/s
- Support of the MFIN / MFOUT
- Additional power supply to directly supply the smart card IC connected via MFIN / MFOUT
- Supported host interfaces

  - SPI interface up to 10 Mbit/s
  - I^{2}C interface up to 400 kbit/s in Fast mode, up to 3400 kbit/s in High-speed mode
  - serial UART in different transfer speeds up to 1228.8 kbit/s, framing according to the RS232 interface with voltage levels according pad voltage supply
- Comfortable 64 byte send and receive FIFO-buffer
- Flexible interrupt modes
- Hard reset with low power function
- Power-down mode per software
- Programmable timer
- Internal oscillator to connect 27.12 MHz quartz
- 2.5 - 3.3 V power supply
- CRC Co-processor
- Free programmable I/O pins
- Internal self test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
AV_{DD}	Supply Voltage	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V, $PV_{DD} \leq AV_{DD} = DV_{DD} = TV_{DD}$	[1][2]	2.5	-	3.6	V
DV_{DD}			[1][2]				
TV_{DD}			[1][2]				
PV_{DD}	Pad power supply	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V, $PV_{DD} \leq AV_{DD} = DV_{DD} = TV_{DD}$	[3]	1.6	-	3.6	V
SV_{DD}	MFIN/MFOUT Pad Power Supply	$AV_{SS} = DV_{SS} = PV_{SS} = TV_{SS} = 0$ V,		1.6	-	3.6	V
I_{HPD}	Hard Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, N_{RESET} = LOW	[4]	-	-	5	µA
I_{SPD}	Soft Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, RF level detector on	[4]	-	-	10	µA
I_{DVDD}	Digital Supply Current	$DV_{DD} = 3$ V		-	6.5	9	mA
I_{AVDD}	Analog Supply Current	$AV_{DD} = 3$ V, bit RCVOff = 0		-	7	10	mA
$I_{AVDD,RCVOFF}$	Analog Supply Current, receiver switched off	$AV_{DD} = 3$ V, bit RCVOff = 1		-	3	5	mA
I_{PVDD}	Pad Supply Current		[2]	-	-	40	mA
I_{TVDD}	Transmitter Supply Current	Continuous Wave	[1][3][8]	-	60	100	mA
T_{amb}	operating ambient temperature			-25		+85	°C

[1] Supply voltage below 3 V reduces the performance (e.g. the achievable operating distance).

[2] AV_{DD}, DV_{DD} and TV_{DD} shall always be on the same voltage level.

[3] PV_{DD} shall always be on the same or lower voltage level than DV_{DD}.

[4] I_{TVDD} depends on TV_{DD} and the external circuitry connected to Tx1 and Tx2

[5] I_{PVDD} depends on the overall load at the digital pins.

[6] During operation with a typical circuitry the overall current is below 100 mA.

[7] I_{SPD} and I_{HPD} are the total currents over all supplies.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between TX1 and TX2 at 13.56 MHz

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
MFRC52201HN1/TRAYB (delivered in 1 Tray)	HVQFN32	see Package Outline in Figure 33 “Package outline package version (HVQFN32)” see Packing Information in Figure 34 “Packing Information 1 Tray”	SOT617-1
MFRC52201HN1/TRAYBM (delivered in 5 Tray)	HVQFN32	see Package Outline in Figure 33 “Package outline package version (HVQFN32)” see Packing Information in Figure 35 “Packing Information 5Tray”	SOT617-1

6. Block diagram

The Analog interface handles the modulation and demodulation of the analog signals.

The contactless UART handles the protocol requirements for the communication schemes in co-operation with the host. The comfortable FIFO buffer allows a fast and convenient data transfer from the host to the contactless UART and vice versa.

Various host interfaces are implemented to fulfil different customer requirements.

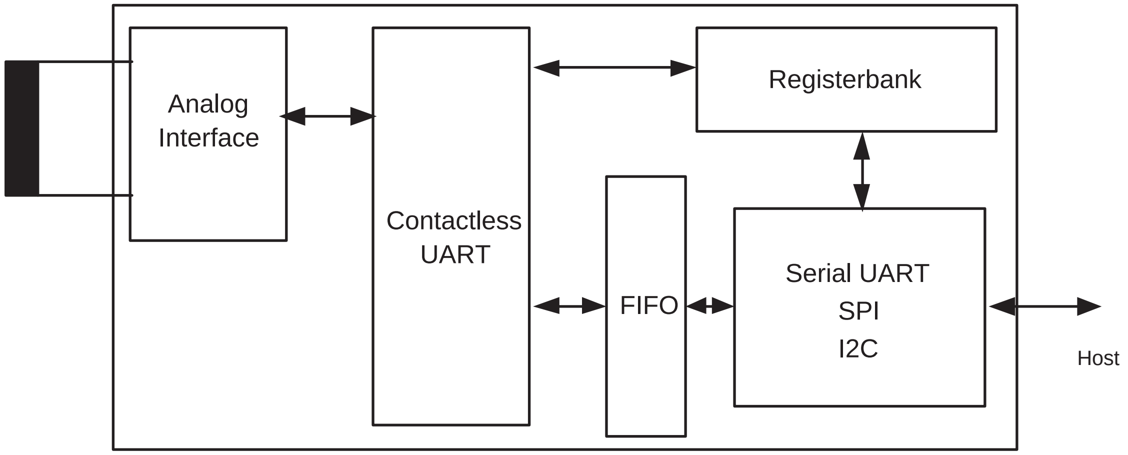

Fig 1. Simplified MFRC522 Block diagram

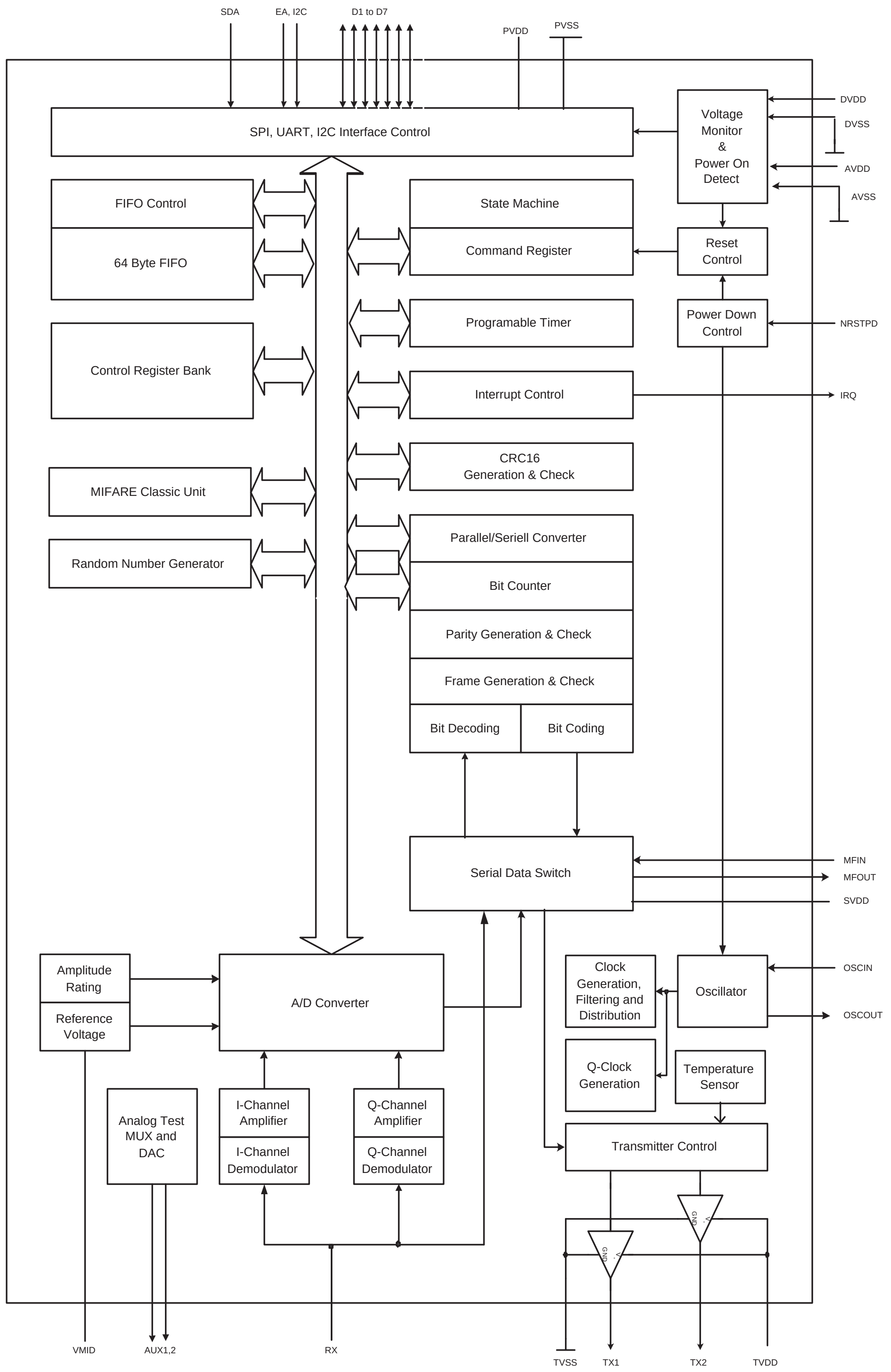

Fig 2. MFRC522 Block diagram

7. Pinning information

7.1 Pinning

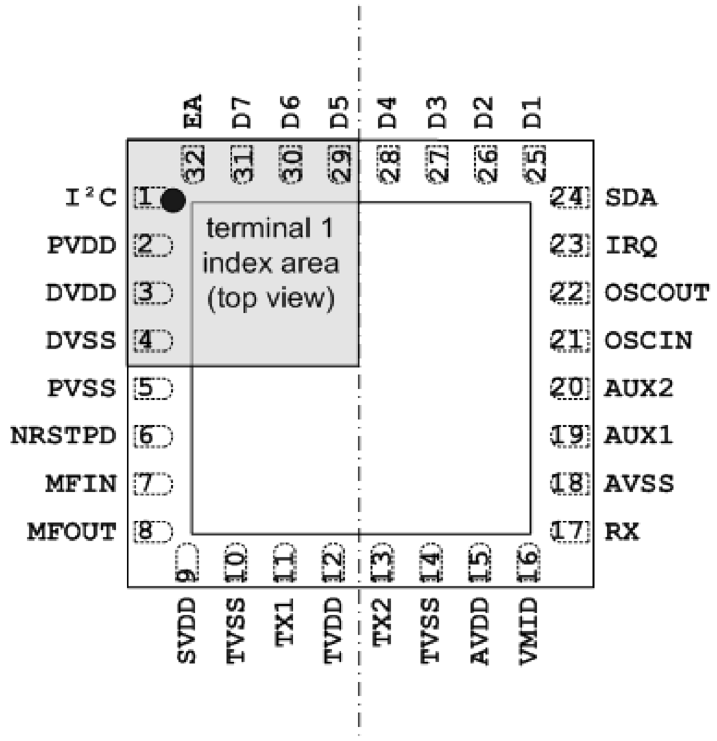

Fig 3. Pinning configuration HVQFN32 (SOT617-1).

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
I²C	1	I	**I2C enable**[2]
PVDD	2	PWR	**Pad power supply**
DVDD	3	PWR	**Digital Power Supply**
DVSS	4	PWR	**Digital Ground**[1]
PVSS	5	PWR	**Pad power supply ground**
NRSTPD	6	I	**Not Reset and Power-down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
MFIN	7	I	**Mifare Signal Input**
MFOUT	8	O	**Mifare Signal Output**
SVDD	9	PWR	**MFIN / MFOUT Pad Power Supply**: provides power to for the MFIN / MFOUT pads
TVSS	10, 14	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2

Table 3: Pin description *…continued*

Symbol	Pin	Type	Description
TX1	11	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
TVDD	12	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
TX2	13	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
TVSS	10, 14	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
AVDD	15	PWR	**Analog Power Supply**
VMID	16	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
RX	17	I	**Receiver Input.** Pin for the received RF signal.
AVSS	18	PWR	**Analog Ground**
AUX1	19	O	**Auxiliary Outputs:** These pins are used for testing.
AUX2	20	O	
OSCIN	21	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHz).
OSCOUT	22	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
IRQ	23	O	**Interrupt Request:** output to signal an interrupt event
SDA	24	I	**Serial Data Line**[2]
D1	25	I/O	**Data Pins for different interfaces** (test port, I^2C, SPI, UART)[2]
D2	26	I/O	
D3	27	I/O	
D4	28	I/O	
D5	29	I/O	
D6	30	I/O	
D7	31	I/O	
EA	32	I	**External Address:** This Pin is used for coding I2C Address[2]

[1] Connection of heat sink pad on package buttom side is not necessary. Optional connection to DVSS is possible.

[2] The pin functionality for the interfaces is explained in Section 10 “DIGITAL Interfaces”.

8. Functional description

MFRC522 transmission module supports the Reader/Writer mode for ISO/IEC 14443A/MIFARE$^{®}$ with different transfer speeds and modulation schemes.

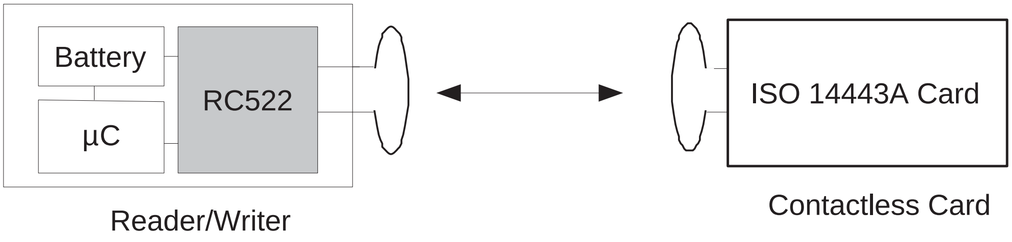

Fig 4. MFRC522 Reader/Writer mode.

The following diagram Figure 5 “ISO/IEC 14443A/MIFARE$^{®}$ Reader/Writer mode communication diagram.” describes the communication on a physical level.

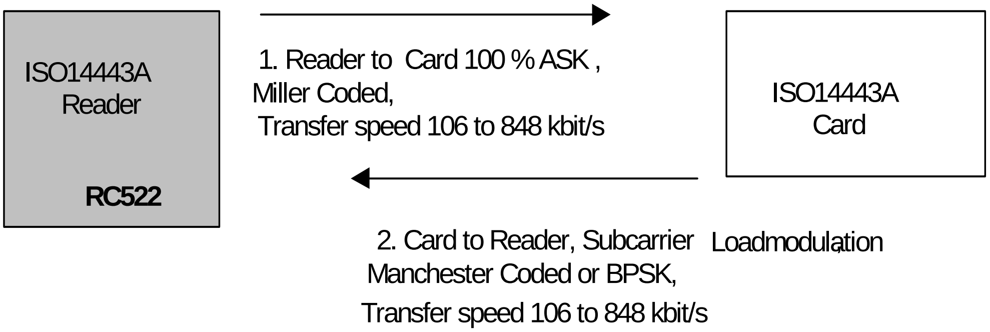

Fig 5. ISO/IEC 14443A/MIFARE$^{®}$ Reader/Writer mode communication diagram.

The communication overview in Table 4 “Communication overview for ISO/IEC 14443A/MIFARE$^{®}$ reader/writer” describes the physical parameters.

Table 4: Communication overview for ISO/IEC 14443A/MIFARE$^{®}$ reader/writer

Communication direction		**ISO/IEC 14443A/ MIFARE$^{®}$**			
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
Reader → Card (send data from the MFRC522 to a card)	Modulation on reader side	100% ASK	100% ASK	100% ASK	100% ASK
	bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
	Bitlength	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs

Table 4: Communication overview for ISO/IEC 14443A/MIFARE® reader/writer *…continued*

Communication direction		**ISO/IEC 14443A/ MIFARE®**			
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
Card → Reader (MFRC522 receives data from a card)	modulation on card side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56MHz/16	13.56MHz/16	13.56MHz/16
	bit coding	Manchester coding	BPSK	BPSK	BPSK

The contactless UART of MFRC522 and a dedicated external host are required to handle the complete MIFARE® / ISO/IEC 14443A / MIFARE® protocol. The following Figure 6 "Data Coding and framing according to ISO/IEC 14443A." shows the Data Coding and framing according to ISO/IEC 14443A / MIFARE®.

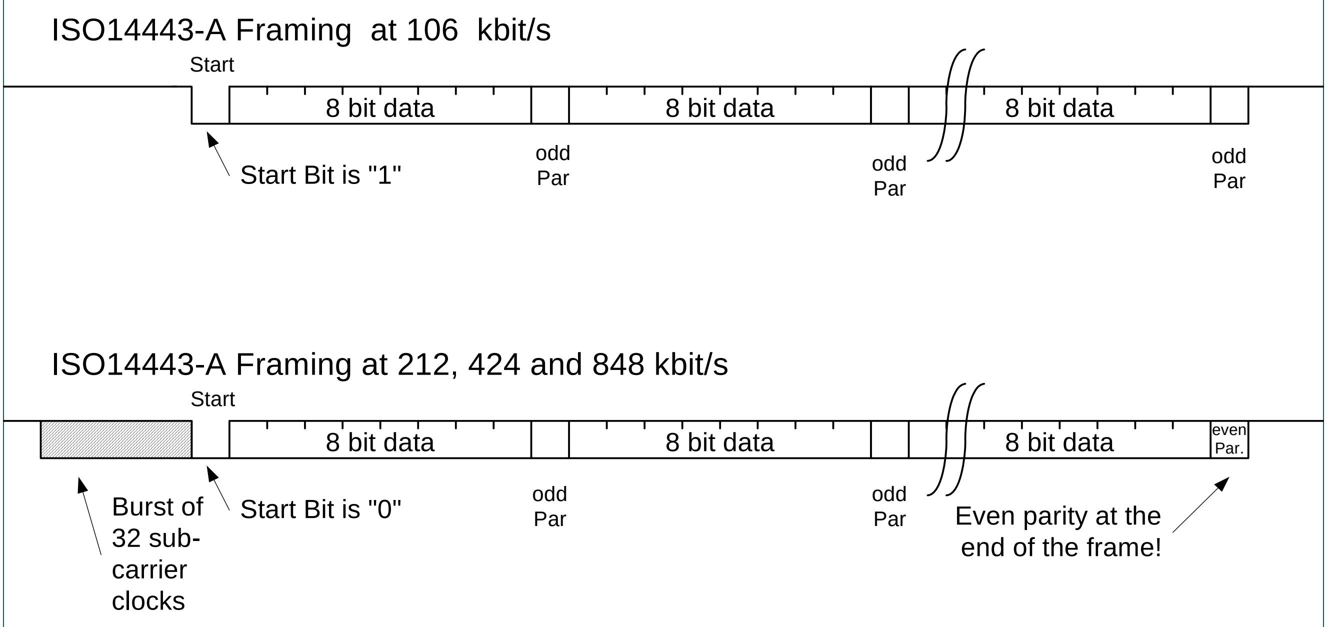

Fig 6. Data Coding and framing according to ISO/IEC 14443A.

The internal CRC co-processor calculates the CRC value according to the definitions given in the ISO/IEC 14443A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off by bit *ParityDisable* in register *0x1D ManualRCVReg*.

9. MFRC522 Register SET

9.1 MFRC522 Registers Overview

Table 5: MFRC522 Registers Overview

Addr (hex)	Register Name	Function
Page 0: Command and Status		
0	Reserved	Reserved for future use
1	CommandReg	Starts and stops command execution
2	ComlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
3	DivlEnReg	Controls bits to enable and disable the passing of Interrupt Requests
4	ComIrqReg	Contains Interrupt Request bits
5	DivIrqReg	Contains Interrupt Request bits
6	ErrorReg	Error bits showing the error status of the last command executed
7	Status1Reg	Contains status bits for communication
8	Status2Reg	Contains status bits of the receiver and transmitter
9	FIFODataReg	In- and output of 64 byte FIFO buffer
A	FIFOLevelReg	Indicates the number of bytes stored in the FIFO
B	WaterLevelReg	Defines the level for FIFO under- and overflow warning
C	ControlReg	Contains miscellaneous Control Registers
D	BitFramingReg	Adjustments for bit oriented frames
E	CollReg	Bit position of the first bit collision detected on the RF-interface
F	Reserved	Reserved for future use
Page 1: Command		
0	Reserved	Reserved for future use
1	ModeReg	Defines general modes for transmitting and receiving
2	TxModeReg	Defines the transmission data rate and framing
3	RxModeReg	Defines the receive data rate and framing
4	TxControlReg	Controls the logical behavior of the antenna driver pins TX1 and TX2
5	TxASKReg	Controls the setting of the TX modulation
6	TxSelReg	Selects the internal sources for the antenna driver
7	RxSelReg	Selects internal receiver settings
8	RxThresholdReg	Selects thresholds for the bit decoder
9	DemodReg	Defines demodulator settings
A	Reserved	Reserved for future use
B	Reserved	Reserved for future use
C	MfTxReg	Controls some MIFARE® communication transmit parameters
D	MfRxReg	Controls some MIFARE® communication receive parameters
E	Reserved	Reserved for future use
F	SerialSpeedReg	Selects the speed of the serial UART interface
Page 2: CFG		
0	Reserved	Reserved for future use

Table 5: MFRC522 Registers Overview *…continued*

Addr (hex)	Register Name	Function
1	CRCResultReg	Shows the actual MSB and LSB values of the CRC calculation
2		
3	Reserved	Reserved for future use
4	ModWidthReg	Controls the setting of the ModWidth
5	Reserved	Reserved for future use
6	RFCfgReg	Configures the receiver gain
7	GsNReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation
8	CWGsPReg	
9	ModGsPReg	
A	TModeReg TPrescalerReg	Defines settings for the internal timer
B		
C	TReloadReg	Describes the 16 bit timer reload value
D		
E	TCounterValReg	Shows the 16 bit actual timer value
F		
Page 3: TestRegister		
0	Reserved	Reserved for future use
1	TestSel1Reg	General test signal configuration
2	TestSel2Reg	General test signal configuration and PRBS control
3	TestPinEnReg	Enables pin output driver on D1-D7
4	TestPinValueReg	Defines the values for D1 - D7 when it is used as I/O bus
5	TestBusReg	Shows the status of the internal testbus
6	AutoTestReg	Controls the digital selftest
7	VersionReg	Shows the version
8	AnalogTestReg	Controls the pins AUX1 and AUX2
9	TestDAC1Reg	Defines the test value for the TestDAC1
A	TestDAC2Reg	Defines the test value for the TestDAC2
B	TestADCReg	Shows the actual value of ADC I and Q
C-F	Reserved	Reserved for production tests

9.1.1 Register Bit Behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle bits with same behavior are grouped in common registers. In Table 6 the access conditions are described.

Table 6: Behavior of Register Bits and its Designation

Abbreviation	Behavior	Description
r/w	read and write	These bits can be written and read by the μ-Controller. Since they are used only for control means, there content is not influenced by internal state machines, e.g. the *ComIEnReg*-Register may be written and read by the μ-Controller. It will also be read by internal state machines, but never changed by them.
dy	dynamic	These bits can be written and read by the μ-Controller. Nevertheless, they may also be written automatically by internal state machines, e.g. the Command-Register changes its value automatically after the execution of the actual command.
r	read only	These register bits hold values which are determined by internal states only, e.g. the *CRCReady* bit can not be written from external but shows internal states.
w	write only	Reading these register bits returns always ZERO.
RFU	-	These registers are reserved for future use and shall not be changed. In case of a write access, it is recommended to write always the value “0”.
RFT	-	These register bits are reserved for future use or production test and shall not be changed.

9.2 Register Description

9.2.1 Page 0: Command and Status

9.2.1.1 Reserved

Functionality is reserved for further use.

Table 7: Reserved register (address 00h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 8: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.1.2 CommandReg

Starts and stops command execution.

Table 9: CommandReg register (address 01h); reset value: 20h

Bit	7	6	5	4	3	2	1	0
Symbol	-		RcvOff	Power Down	Command			
Access Rights	RFU		r/w	dy	dy			

Table 10: Description of CommandReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5	RcvOff	Set to logic 1, the analog part of the receiver is switched off.
4	PowerDown	Set to logic 1, Soft Power-down mode is entered. Set to logic 0, the MFRC522 starts the wake up procedure. During this procedure this bit still shows a logic 1. A logic 0 indicates that the MFRC522 is ready for operations; see Section 16.2 “Soft Power-down”. **Remark:** The bit PowerDown cannot be set, when the command SoftReset has been activated.
3 to 0	Command	Activates a command according to the Command Code. Reading this register shows which command is actually executed (see Section 18.3 “MFRC522 Commands Overview”).

9.2.1.3 CommIEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 11: CommIEnReg register (address 02h); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 12: Description of CommIEnReg bits

Bit	Symbol	Description
7	IRqInv	Set to logic 1, the signal on pin IRQ is inverted with respect to bit *IRq* in the register *Status1Reg*. Set to logic 0, the signal on pin IRQ is equal to bit *IRq*. In combination with bit *IRqPushPull* in register *DivIEnReg*, the default value of logic 1 ensures, that the output level on pin IRQ is tristate.
6	TxIEn	Allows the transmitter interrupt request (indicated by bit *TxIRq*) to be propagated to pin IRQ.
5	RxIEn	Allows the receiver interrupt request (indicated by bit *RxIRq*) to be propagated to pin IRQ.
4	IdleIEn	Allows the idle interrupt request (indicated by bit *IdleIRq*) to be propagated to pin IRQ.
3	HiAlertIEn	Allows the high alert interrupt request (indicated by bit *HiAlertIRq*) to be propagated to pin IRQ.

Table 12: Description of CommIEnReg bits

Bit	Symbol	Description
2	LoAlertIEn	Allows the low alert interrupt request (indicated by bit *LoAlertIRq*) to be propagated to pin IRQ.
1	ErrIEn	Allows the error interrupt request (indicated by bit *ErrIRq*) to be propagated to pin IRQ.
0	TimerIEn	Allows the timer interrupt request (indicated by bit *TimerIRq*) to be propagated to pin IRQ.

9.2.1.4 DivIEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 13: DivIEnReg register (address 03h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	IRQPushPull	-		MfinActIEn	-	CRCIEn	-	
Access Rights	r/w	RFU		r/w	RFU	r/w	RFU	

Table 14: Description of DivIEnReg bits

Bit	Symbol	Description
7	IRQPushPull	Set to logic 1, the pin IRQ works as standard CMOS output pad. Set to logic 0, the pin IRQ works as open drain output pad.
6 to 5	-	Reserved for future use.
4	MfinActIEn	Allows the MFIN active interrupt request to be propagated to pin IRQ.
3	-	Reserved for future use.
2	CRCIEn	Allows the CRC interrupt request (indicated by bit *CRCIRq*) to be propagated to pin IRQ.
1 to 0	-	Reserved for future use.

9.2.1.5 CommIRqReg

Contains Interrupt Request bits.

Table 15: CommIRqReg register (address 04h); reset value: 14h

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access Rights	w	dy	dy	dy	dy	dy	dy	dy

Table 16: Description of CommIRqReg bits
All bits in the register CommIRqReg shall be cleared by software.

Bit	Symbol	Description
7	Set1	Set to logic 1, *Set1* defines that the marked bits in the register *CommIRqReg* are set. Set to logic 0, *Set1* defines, that the marked bits in the register *CommIRqReg* are cleared.
6	TxIRq	Set to logic 1 immediately after the last bit of the transmitted data was sent out.
5	RxIRq	Set to logic 1 when the receiver detects the end of a valid data stream. If the bit *RxNoErr* in register *RxModeReg* is set to logic 1, Bit *RxIRq* is only set to logic 1 when data bytes are available in the FIFO.
4	IdleIRq	Set to logic 1, when a command terminates by itself e.g. when the *CommandReg* changes its value from any command to the Idle Command. If an unknown command is started, the *CommandReg* changes its content to the idle state and the bit *IdleIRq* is set. Starting the Idle Command by the μ-Controller does not set bit *IdleIRq*.
3	HiAlertIRq	Set to logic 1, when bit *HiAlert* in register *Status1Reg* is set. In opposition to *HiAlert*, *HiAlertIRq* stores this event and can only be reset as indicated by bit *Set1*.

Table 16: Description of CommIRqReg bits *…continued*

All bits in the register CommIRqReg shall be cleared by software.

Bit	Symbol	Description
2	LoAlertIRq	Set to logic 1, when bit *LoAlert* in register *Status1Reg* is set. In opposition to *LoAlert*, *LoAlertIRq* stores this event and can only be reset as indicated by bit *Set1*.
1	ErrIRq	Set to logic 1 if any error bit in the *ErrorReg* Register is set.
0	TimerIRq	Set to logic 1 when the timer decrements the *TimerValue* Register to zero.

9.2.1.6 DivIRqReg

Contains Interrupt Request bits

Table 17: DivIRqReg register (address 05h); reset value: X0h

Bit	7	6	5	4	3	2	1	0
Symbol	Set2	-		MfinActIRq	-	CRCIRq	-	
Access Rights	w	RFU		dy	RFU	dy	RFU	

Table 18: Description of DivIRqReg bits

All bits in the register DivIRqReg shall be cleared by software.

Bit	Symbol	Description
7	Set2	Set to logic 1, *Set2* defines that the marked bits in the register *DivIRqReg* are set. Set to logic 0, *Set2* defines, that the marked bits in the register *DivIRqReg* are cleared
6 to 5	-	Reserved for future use.
4	MfinActIRq	Set to logic 1, when MFIN is active. This interrupt is set when either a rising or falling signal edge is detected.
3	-	Reserved for future use.
2	CRCIRq	Set to logic 1, when the CRC command is active and all data are processed.
1 to 0	-	Reserved for future use.

9.2.1.7 ErrorReg

Error bit register showing the error status of the last command executed.

Table 19: ErrorReg register (address 06h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	-	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access Rights	r	r	RFU	r	r	r	r	r

Table 20: Description of ErrorReg bits

Bit	Symbol	Description
7	WrErr	Set to logic 1, when data is written into the FIFO by the host during the MFAuthent command or if data is written into the FIFO by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface.
6	TempErr[1]	Set to logic 1, if the internal temperature sensor detects overheating. In this case, the antenna drivers are switched off automatically.
5	-	Reserved for future use.
4	BufferOvfl	Set to logic 1, if the host or a MFRC522’s internal state machine (e.g. receiver) tries to write data into the FIFO buffer although the FIFO buffer is already full.
3	CollErr	Set to logic 1, if a bit-collision is detected. It is cleared automatically at receiver start-up phase. This bit is only valid during the bitwise anticollision at 106 kbit/s. During communication schemes at 212, 424 and 848 kbit/s this bit is always set to logic 0.
2	CRCErr	Set to logic 1, if bit *RxCRCEn* in register *RxModeReg* is set and the CRC calculation fails. It is cleared to logic 0 automatically at receiver start-up phase.
1	ParityErr	Set to logic 1, if the parity check has failed. It is cleared automatically at receiver start-up phase. Only valid for ISO/IEC 14443A/MIFARE® communication at 106 kbit/s.
0	ProtocolErr	Set to logic 1, if one out of the following cases occur: • Set to logic 1 if the SOF is incorrect. It is cleared automatically at receiver start-up phase. The bit is only valid for 106 kbit/s. • During the MFAuthent Command, bit *ProtocolErr* is set to logic 1, if the number of bytes received in one data stream is incorrect.

[1] Command execution will clear all error bits except for bit TempErr. A setting by software is impossible.

9.2.1.8 Status1Reg

Contains status bits of the CRC, Interrupt and FIFO buffer.

Table 21: Status1Reg register (address 07h); reset value: 21h

Bit	7	6	5	4	3	2	1	0
Symbol	-	CRCOk	CRCReady	IRq	TRunning	-	HiAlert	LoAlert
Access Rights	RFU	r	r	r	r	RFU	r	r

Table 22: Description of Status1Reg bits

Bit	Symbol	Description
7	-	Reserved for future use.
6	CRCOk	Set to logic 1, if the CRC result is zero. For data transmission and reception the bit *CRCOk* is undefined (use *CRCErr* in register *ErrorReg*). *CRCOk* indicates the status of the CRC co-processor, during calculation the value changes to logic 0, when the calculation is done correctly, the value changes to logic 1.
5	CRCReady	Set to logic 1, when the CRC calculation has finished. This bit is only valid for the CRC co-processor calculation using the command CalcCRC.
4	IRq	This bit shows, if any interrupt source requests attention (with respect to the setting of the interrupt enable bits, see register *CommIEnReg* and *DivIEnReg*).
3	TRunning	Set to logic 1, if the MFRC522’s timer unit is running, e.g. the timer will decrement the *TCounterValReg* with the next timer clock. **Remark:** In the gated mode the bit TRunning is set to logic 1, when the timer is enabled by the register bits. This bit is not influenced by the gated signal.
2	-	Reserved for future use.
1	HiAlert	Set to logic 1, when the number of bytes stored in the FIFO buffer fulfils the following equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ Example: FIFOLength = 60, WaterLevel = 4 → HiAlert = 1 FIFOLength = 59, WaterLevel = 4 → HiAlert = 0
0	LoAlert	Set to logic 1, when the number of bytes stored in the FIFO buffer fulfils the following equation: $LoAlert = FIFOLength \leq WaterLevel$ Example: FIFOLength = 4, WaterLevel = 4 → LoAlert = 1 FIFOLength = 5, WaterLevel = 4 → LoAlert = 0

9.2.1.9 Status2Reg

Contains status bits of the receiver, transmitter and data mode detector.

Table 23: Status2Reg register (address 08h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	TempSens Clear	I^{2}CForceHS	-		MFCrypto1On	Modem State		
Access Rights	r/w	r/w	RFU		dy	r		

Table 24: Description of Status2Reg bits

Bit	Symbol	Description
7	TempSensClear	Set to logic 1, this bit clears the temperature error, if the temperature is below the alarm limit of 125 °C.
6	I^{2}CForceHS	I^{2}C input filter settings. Set to logic 1, the I^{2}C input filter is set to the High-speed mode independent of the I^{2}C protocol. Set to logic 0, the I^{2}C input filter is set to the used I^{2}C protocol.
5 to 4	-	Reserved for future use.
3	MFCrypto1On	This bit indicates that the MIFARE® Crypto1 unit is switched on and therefore all data communication with the card is encrypted. This bit can only be set to logic 1 by a successful execution of the MFAuthent Command. This bit is only valid in Reader/Writer mode for MIFARE® Standard cards. This bit shall be cleared by software.
2 to 0	Modem State	ModemState shows the state of the transmitter and receiver state machines. Status Description 000 IDLE 001 Wait for bit *StartSend* in register *BitFramingReg* 010 TxWait: Wait until Rf field is present, if the bit *TxWaitRF* is set to logic 1. The minimum time for TxWait is defined by the *TxWaitReg* register. 011 Transmitting 100 RxWait: Wait until RF field is present, if the bit *RxWaitRF* is set to logic 1. The minimum time for RxWait is defined by the *RxWaitReg* register. 101 Wait for data 110 Receiving

9.2.1.10 FIFODataReg

In- and output of 64 byte FIFO buffer.

Table 25: FIFODataReg register (address 09h); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData							
Access Rights	dy							

Table 26: Description ofFIFODataReg bits

Bit	Symbol	Description
7 to 0	FIFOData	Data input and output port for the internal 64 byte FIFO buffer. The FIFO buffer acts as parallel in/parallel out converter for all serial data stream in- and outputs.

9.2.1.11 FIFOLevelReg

Indicates the number of bytes stored in the FIFO.

Table 27: FIFOLevelReg register (address 0Ah); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	FlushBuffer	FIFOLevel						
Access Rights	w	r						

Table 28: Description of FIFOLevelReg bits

Bit	Symbol	Description
7	FlushBuffer	Set to logic 1, this bit clears the internal FIFO-buffer’s read- and write-pointer and the bit *BufferOvfl* in the register *ErrReg* immediately. Reading this bit will always return 0.
6 to 0	FIFOLevel	Indicates the number of bytes stored in the FIFO buffer. Writing to the *FIFODataReg* increments, reading decrements the *FIFOLevel*.

9.2.1.12 WaterLevelReg

Defines the level for FIFO under- and overflow warning.

Table 29: WaterLevelReg register (address 0Bh); reset value: 08h

Bit	7	6	5	4	3	2	1	0
Symbol	-		WaterLevel					
Access Rights	RFU		r/w					

Table 30: Description of WaterLevelReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	WaterLevel	This register defines a warning level to indicate a FIFO-buffer over- or underflow: The bit *HiAlert* in *Status1Reg* is set to logic 1, if the remaining number of bytes in the FIFO-buffer space is equal or less than the defined number of *WaterLevel* bytes. The bit *LoAlert* in *Status1Reg* is set to logic 1, if equal or less than *WaterLevel* bytes are in the FIFO. **Remark:** For the calculation of *HiAlert* and *LoAlert* see Section 9.2.1.8 “Status1Reg”.

9.2.1.13 ControlReg

Miscellaneous control bits.

Table 31: ControlReg register (address 0Ch); reset value: 10h

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow	-			RxLastBits		
Access Rights	w	w	RFU			r		

Table 32: Description of ControlReg bits

Bit	Symbol	Description
7	TStopNow	Set to logic 1, the timer stops immediately. Reading this bit will always return 0.
6	TStartNow	Set to logic 1 starts the timer immediately. Reading this bit will always return 0.
5 to 3	-	Reserved for future use.
2 to 0	RxLastBits	Shows the number of valid bits in the last received byte. If 0, the whole byte is valid.

9.2.1.14 BitFramingReg

Adjustments for bit oriented frames.

Table 33: BitFramingReg register (address 0Dh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend	RxAlign			-	TxLastBits		
Access Rights	w	r/w			RFU	r/w		

Table 34: Description of BitFramingReg bits

Bit	Symbol	Description
7	StartSend	Set to logic 1, the transmission of data starts. This bit is only valid in combination with the Transceive command.
6 to 4	RxAlign	Used for reception of bit oriented frames: *RxAlign* defines the bit position for the first bit received to be stored in the FIFO. Further received bits are stored at the following bit positions.
		Example: RxAlign = 0: the LSB of the received bit is stored at bit 0, the second received bit is stored at bit position 1. RxAlign = 1: the LSB of the received bit is stored at bit 1, the second received bit is stored at bit position 2. RxAlign = 7: the LSB of the received bit is stored at bit 7, the second received bit is stored in the following byte at bit position 0.
		This bits shall only be used for bitwise anticollision at 106 kbit/s. In all other modes it shall be set to 0.
3	-	Reserved for future use.
2 to 0	TxLastBits	Used for transmission of bit oriented frames: *TxLastBits* defines the number of bits of the last byte that shall be transmitted. A 000b indicates that all bits of the last byte shall be transmitted.

9.2.1.15 CollReg

Defines the first bit collision detected on the RF interface.

Table 35: CollReg register (address 0Eh); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	Values AfterColl	-	CollPos NotValid	CollPos				
Access Rights	r/w	RFU	r	r				

Table 36: Description of CollReg bits

Bit	Symbol	Description
7	ValuesAfterColl	If this bit is set to logic 0, all receiving bits will be cleared after a collision. This bit shall only be used during bitwise anticollision at 106 kbit/s, otherwise it shall be set to logic 1.
6	-	Reserved for future use.
5	CollPosNotValid	Set to logic 1, if no collision is detected or the position of the collision is out of the range of bits *CollPos*.

Table 36: Description of CollReg bits

Bit	Symbol	Description
4 to 0	CollPos	These bits show the bit position of the first detected collision in a received frame. Only data bits are interpreted.
		Example: 00h indicates a bit collision in the 32nd bit 01h indicates a bit collision in the 1st bit 08h indicates a bit collision in the 8th bit
		These bits shall only be interpreted if bit *CollPosNotValid* is set to logic 0.

9.2.1.16 Reserved

Functionality is reserved for further use.

Table 37: Reserved register (address 0Fh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 38: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

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9.2.2.1 Reserved

Functionality is reserved for further use.

Table 39: Reserved register (address 10h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 40: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.2.2 ModeReg

Defines general mode settings for transmitting and receiving.

Table 41: ModeReg register (address 11h); reset value: 3Fh

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	-	TxWaitRF	-	PolMFin	-	CRCPreset	
Access Rights	r/w	RFU	r/w	RFU	r/w	RFU	r/w	

Table 42: Description of ModeReg bits

Bit	Symbol	Description
7	MSBFirst	Set to logic 1, the CRC co-processor calculates the CRC with MSB first and the *CRCResultMSB* and the *CRCResultLSB* in the *CRCResultReg* register are bit reversed. **Remark:** During RF communication this bit is ignored.
6	-	Reserved for future use.
5	TxWaitRF	Set to logic 1 the transmitter can only be started, if an RF field is generated.
4	-	Reserved for future use.
3	PolMFin	PolMFin defines the polarity of the MFIN pin. Set to logic 1, the polarity of MFIN pin is active high. Set to logic 0 the polarity of MFIN pin is active low. **Remark:** The internal envelope signal is coded active low. Changing this bit will generate a MFinActIRq event.
2	-	Reserved for future use.
1 to 0	CRCPreset	Defines the preset value for the CRC co-processor for the command CalCRC. **Remark:** During any communication, the preset values is selected automatically according to the definition in the bits in RxModeReg and TxModeReg. **Value** **Description** 00 0000 01 6363 10 A671 11 FFFF

9.2.2.3 TxModeReg

Defines the data rate during transmission.

Table 43: TxModeReg register (address 12h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	TxCRCEn	TxSpeed			InvMod	-		
Access Rights	r/w	dy			r/w	RFU		

Table 44: Description of TxModeReg bits

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>TxCRCEn</td><td>Set to logic 1, this bit enables the CRC generation during data transmission.
Remark: This bit shall only be set to logic 0 at 106 kbit/s.</td></tr>
<tr><td>6 to 4</td><td>TxSpeed</td><td>Defines the bit rate while data transmission. The MFRC522 handels transfer speeds up to 848 kbit/s.
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>000</td><td>106 kbit/s</td></tr>
<tr><td>001</td><td>212 kbit/s</td></tr>
<tr><td>010</td><td>424 kbit/s</td></tr>
<tr><td>011</td><td>848 kbit/s</td></tr>
<tr><td>100</td><td>Reserved</td></tr>
<tr><td>101</td><td>Reserved</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3</td><td>InvMod</td><td>Set to logic 1, the modulation for transmitting data is inverted.</td></tr>
<tr><td>2 to 0</td><td>-</td><td>Reserved for future use.</td></tr>
</table>

9.2.2.4 RxModeReg

Defines the data rate during reception.

Table 45: RxModeReg register (address 13h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	RxCRCEn	RxSpeed			RxNoErr	RxMultiple	-	
Access Rights	r/w	dy			r/w	r/w	RFU	

Table 46: Description of RxModeReg bits

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>RxCRCEn</td><td>Set to logic 1, this bit enables the CRC calculation during reception.
Remark: This bit shall only be set to logic 0 at 106 kbit/s.</td></tr>
<tr><td>6 to 4</td><td>RxSpeed</td><td>Defines the bit rate while data receiving. The MFRC522 handles transfer speeds up to 848kbit/s.
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>000</td><td>106 kbit/s</td></tr>
<tr><td>001</td><td>212 kbit/s</td></tr>
<tr><td>010</td><td>424 kbit/s</td></tr>
<tr><td>011</td><td>848 kbit/s</td></tr>
<tr><td>100</td><td>Reserved</td></tr>
<tr><td>101</td><td>Reserved</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Table 46: Description of RxModeReg bits *...continued*

Bit	Symbol	Description
3	RxNoErr	If set to logic 1, a not valid received data stream (less than 4 bits received) will be ignored. The receiver will remain active.
2	RxMultiple	Set to logic 0, the receiver is deactivated after receiving a data frame. Set to logic 1, it is possible to receive more than one data frame. This bit is only valid for data rates above 106 kbit/s to handle the Polling command. Having set this bit, the receive and transceive commands will not terminate automatically. In this case the multiple receiving can only be deactivated by writing any command (except the Receive command) to the CommandReg register or by clearing the bit by the host. If set to logic 1, at the end of a received data stream an error byte is added to the FIFO. The error byte is a copy of the *ErrorReg* register.
1 to 0	-	Reserved for future use.

9.2.2.5 TxControlReg

Controls the logical behavior of the antenna driver pins Tx1 and Tx2.

Table 47: TxControlReg register (address 14h); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	InvTx2RF On	InvTx1RF On	InvTx2RF Off	InvTx1RF Off	Tx2CW	-	Tx2RFEn	Tx1RFEn
Access Rights	r/w	r/w	r/w	r/w	r/w	RFU	r/w	r/w

Table 48: Description of TxControlReg bits

Bit	Symbol	Description
7	InvTx2RFOn	Set to logic 1, the output signal at pin TX2 will be inverted, if driver TX2 is enabled.
6	InvTx1RFOn	Set to logic 1, the output signal at pin TX1 will be inverted, if driver TX1 is enabled.
5	InvTx2RFOff	Set to logic 1, the output signal at pin TX2 will be inverted, if driver TX2 is disabled.
4	InvTx1RFOff	Set to logic 1, the output signal at pin TX1 will be inverted, if driver TX1 is disabled.
3	Tx2CW	Set to logic 1, the output signal on pin TX2 will deliver continuously the un-modulated 13.56 MHz energy carrier. Set to logic 0, *Tx2CW* is enabled to modulate the 13.56 MHz energy carrier.
2	-	Reserved for future use.
1	Tx2RFEn	Set to logic 1, the output signal on pin TX2 will deliver the 13.56 MHz energy carrier modulated by the transmission data.
0	Tx1RFEn	Set to logic 1, the output signal on pin TX1 will deliver the 13.56 MHz energy carrier modulated by the transmission data.

9.2.2.6 TxASKReg

Controls the settings of the transmit modulation.

Table 49: TxAutoReg register (address 15h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	Force100ASK	-					
Access Rights	RFU	r/w	RFU					

Table 50: Description of TxAutoReg bits

Bit	Symbol	Description
7	-	Reserved for future use.
6	Force100ASK	Set to logic 1, *Force100ASK* forces a 100% ASK modulation independent of the setting in register *ModGsPReg*.
5 to 0	-	Reserved for future use.

9.2.2.7 TxSelReg

Selects the internal sources for the analog part.

Table 51: TxSelReg register (address 16h); reset value: 10h

Bit	7	6	5	4	3	2	1	0
Symbol	-		DriverSel		MfOutSel			
Access Rights	RFU		r/w		r/w			

Table 52: Description of TxSelReg bits

Bit	Symbol	Description	
7 to 6	-	Reserved for future use.	
5 to 4	DriverSel	Selects the input of driver Tx1 and Tx2.	
		Value	**Description**
		00	Tristate **Remark:** In soft power-down the drivers are only in tristate mode if DriverSel is set to tristate mode.
		01	Modulation signal (envelope) from the internal coder, Miller Pulse Coded.
		10	Modulation signal (envelope) from MIFIN
		11	High **Remark:** The High level depends on the setting of InvTx1RFOn/ InvTx1RFOff and InvTx2RFOn/ InvTx2RFOff.

Table 52: Description of TxSelReg bits

Bit	Symbol	Description	
3 to 0	MFOutSel	Selects the input for the MFOUT Pin.	
		Value	**Description**
		0000	Tristate
		0001	Low
		0010	High
		0011	TestBus signal as defined by bit *TestBusBitSel* in register *TestSel1Reg*.
		0100	Modulation signal (envelope) from the internal coder, Miller Puls Coded
		0101	Serial data stream to be transmitted, data stream before Miller Coder
		0110	Reserved
		0111	Serial data stream received, data stream after Manchester Decoder
		1000-1111	Reserved

9.2.2.8 RxSelReg

Selects internal receiver settings.

Table 53: RxSelReg register (address 17h); reset value: 84h

Bit	7	6	5	4	3	2	1	0
Symbol	UartSel		RxWait					
Access Rights	r/w		r/w					

Table 54: Description of RxSelReg bits

Bit	Symbol	Description	
7 to 6	UartSel	Selects the input of the contactless UART	
		Value	**Description**
		00	Constant Low
		01	Manchester with sub-carrier from MFIN pin
		10	Modulation signal from the internal analog part, default
		11	NRZ coding without sub-carrier from MFIN pin. Only valid for transfer speeds above 106 kbit/s.
5 to 0	RxWait	After data transmission, the activation of the receiver is delayed for *RxWait* bit-clocks. During this 'frame guard time' any signal at pin Rx is ignored.This parameter is ignored by the receive command. All other commands (e.g. Transceive, MFAuthent) use this parameter. The counter starts immediately after the external RF field is switched on.	

9.2.2.9 RxThresholdReg

Selects thresholds for the bit decoder.

Table 55: RxThresholdReg register (address 18h); reset value: 84h

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel				-	CollLevel		
Access Rights	r/w				RFU	r/w		

Table 56: Description of RxThresholdReg bits

Bit	Symbol	Description
7 to 4	MinLevel	Defines the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is not evaluated.
3	-	Reserved for future use.
2 to 0	CollLevel	Defines the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester-coded signal to generate a bit-collision relatively to the amplitude of the stronger half-bit.

9.2.2.10 DemodReg

Defines demodulator settings.

Table 57: DemodReg register (address 19h); reset value: 4Dh

Bit	7	6	5	4	3	2	1	0
Symbol	AddIQ		FixIQ	-	TauRcv		TauSync	
Access Rights	r/w		r/w	RFU	r/w		r/w	

Table 58: Description of DemodReg bits

<table>
<tr><th>Bit</th><th>Symbol</th><th colspan="2">Description</th></tr>
<tr><td>7 to 6</td><td>AddIQ</td><td colspan="2">Defines the use of I and Q channel during reception
Remark: FixIQ has to be set to logic 0 to enable the following settings.</td></tr>
<tr><td></td><td></td><td>**Value**</td><td>**Description**</td></tr>
<tr><td></td><td></td><td>00</td><td>Select the stronger channel</td></tr>
<tr><td></td><td></td><td>01</td><td>Select the stronger channel and freeze the selected during communication</td></tr>
<tr><td></td><td></td><td>10</td><td>Reserved</td></tr>
<tr><td></td><td></td><td>11</td><td>Reserved</td></tr>
<tr><td>5</td><td>FixIQ</td><td colspan="2">If set to logic 1 and the bits *AddIQ* are set to X0b, the reception is fixed to I channel.
If set to logic 1 and the bits *AddIQ* are set to X1b, the reception is fixed to Q channel.</td></tr>
<tr><td>4</td><td>-</td><td colspan="2">Reserved for future use.</td></tr>
<tr><td>3 to 2</td><td>TauRcv</td><td colspan="2">Changes the time constant of the internal PLL during data reception.
Remark: If set to 00b, the PLL is frozen during data reception.</td></tr>
<tr><td>1 to 0</td><td>TauSync</td><td colspan="2">Changes the time constant of the internal PLL during burst.</td></tr>
</table>

9.2.2.11 Reserved

Functionality is reserved for further use.

Table 59: Reserved register (address 1Ah); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 60: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.2.12 Reserved

Functionality is reserved for further use.

Table 61: Reserved register (address 1Bh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 62: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.2.13 MfTxReg

Controls some MIFARE® communication transmit parameters

Table 63: MfTxReg register (address 1Ch); reset value: 62h

Bit	7	6	5	4	3	2	1	0
Symbol	-						TxWait	
Access Rights	RFU						r/w	

Table 64: Description of MifNFCReg bits

Bit	Symbol	Description
7 to 2	-	Reserved for future use.
1 to 0	TxWait	These bits define the additional response time. Per default 7 bits are added to the value of the register bit.

9.2.2.14 MfRxReg

Table 65: MfRxReg register (address 1Dh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-			Parity Disable	-			
Access Rights	RFU			r/w	RFU			

Table 66: Description of ManualRCVReg bits

Bit	Symbol	Description
7 to 5	-	Reserved for future use.
4	Parity Disable	If this bit is set to logic 1, the generation of the Parity bit for transmission and the Parity-Check for receiving is switched off. The received Parity bit is handled like a data bit.
3 to 0	-	Reserved for future use.

9.2.2.15 Reserved

Functionality is reserved for further use.

Table 67: Reserved register (address 1Eh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 68: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.2.16 SerialSpeedReg

Selects the speed of the serial UART interface.

Table 69: SerialSpeedReg register (address 1Fh); reset value: EBh

Bit	7	6	5	4	3	2	1	0
Symbol	BR_T0			BR_T1				
Access Rights	r/w			r/w				

Table 70: Description of SerialSpeedReg bits

Bit	Symbol	Description
7 to 5	BR_T0	Factor BR_T0 to adjust the transfer speed, for description see Section 10.3.2 “Selection of the transfer speeds”.
4 to 0	BR_T1	Factor BR_T1 to adjust the transfer speed, for description see Section 10.3.2 “Selection of the transfer speeds”.

9.2.3 Page 2: Configuration

9.2.3.1 Reserved

Functionality is reserved for further use.

Table 71: Reserved register (address 20h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 72: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.3.2 CRCResultReg

Shows the actual MSB and LSB values of the CRC calculation.

Remark: The CRC is split into two 8-bit register.

Table 73: CRCResultReg register (address 21h); reset value: FFh

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultMSB							
Access Rights	r							

Table 74: Description of CRCResultReg higher bits

Bit	Symbol	Description
7 to 0	CRCResultMSB	This register shows the actual value of the most significant byte of the *CRCResultReg* register. It is valid only if bit *CRCReady* in register *Status1Reg* is set to logic 1.

Table 75: CRCResultReg register (address 22h); reset value: FFh

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultLSB							
Access Rights	r							

Table 76: Description of CRCResultReg lower bits

Bit	Symbol	Description
7 to 0	CRCResultLSB	This register shows the actual value of the least significant byte of the *CRCResult* register. It is valid only if bit *CRCReady* in register *Status1Reg* is set to logic 1.

9.2.3.3 Reserved

Functionality is reserved for further use.

Table 77: Reserved register (address 23h); reset value: 88h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 78: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.3.4 ModWidthReg

Controls the setting of modulation width.

Table 79: ModWidthReg register (address 24h); reset value: 26h

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidth							
Access Rights	r/w							

Table 80: Description of ModWidthReg bits

Bit	Symbol	Description
7 to 0	ModWidth	These bits define the width of the Miller modulation as multiples of the carrier frequency (ModWidth +1/fc). The maximum value is half the bit period.

9.2.3.5 Reserved

Functionality is reserved for further use.

Table 81: Reserved register (address 25h); reset value: 87h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 82: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.3.6 RFCfgReg

Configures the receiver gain.

Table 83: RFCfgReg register (address 26h); reset value: 48h

Bit	7	6	5	4	3	2	1	0
Symbol	-	RxGain			-			
Access Rights	RFU	r/w			RFU			

Table 84: Description of RFCfgReg bits

Bit	Symbol	Description	
7	-	Reserved for future use.	
6 to 4	RxGain	This register defines the receivers signal voltage gain factor:	
		Value	**Description**
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	-	.Reserved for future use.	

9.2.3.7 GsNReg

Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when the driver is switched on.

Table 85: GsNReg register (address 27h); reset value: 88h

Bit	7	6	5	4	3	2	1	0
Symbol	CWGsN				ModGsN			
Access Rights	r/w				r/w			

Table 86: Description of GsNOnReg bits

Bit	Symbol	Description
7 to 4	CWGsN	The value of this register defines the conductance of the output N-driver during times of no modulation. This may be used to regulate the output power and subsequently current consumption and operating distance. **Remark:** The conductance value is binary weighted. During soft Power-down mode the highest bit is forced to 1. This value is only used if the driver TX1 or TX2 are switched on.
3 to 0	ModGsN	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. **Remark:** The conductance value is binary weighted. During soft Power-down mode the highest bit is forced to 1. This value is only used if the driver TX1 or Tx2 are switched on.

9.2.3.8 CWGsPReg

Defines the conductance of the P-driver during times of no modulation

Table 87: CWGsPReg register (address 28h); reset value: 20h

Bit	7	6	5	4	3	2	1	0
Symbol	-		CWGsP					
Access Rights	RFU		r/w					

Table 88: Description of CWGsPReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	CWGsP	The value of this register defines the conductance of the output P-driver. This may be used to regulate the output power and subsequently current consumption and operating distance. **Remark:** The conductance value is binary weighted. During soft Power-down mode the highest bit is forced to 1.

9.2.3.9 ModGsPReg

Defines the driver P-output conductance during modulation.

Table 89: ModGsPReg register (address 29h); reset value: 20h

Bit	7	6	5	4	3	2	1	0
Symbol	-		ModGsP					
Access Rights	RFU		r/w					

Table 90: Description of ModGsPReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	ModGsP	The value of this register defines the conductance of the output P-driver for the time of modulation. This may be used to regulate the modulation index. **Remark:** The conductance value is binary weighted. During soft Power-down mode the highest bit is forced to 1. If Force100ASK is set to logic 1, the value of ModGsP has no effect.

9.2.3.10 TMode Register, TPrescaler Register

Defines settings for the timer.

Remark: The Prescaler value is split over two registers.

Table 91: TModeReg register (address 2Ah); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	TAuto	TGated		TAutoRestart	TPrescaler_Hi			
Access Rights	r/w	r/w		r/w	r/w			

Table 92: Description of TModeReg bits

<table>
<tr><th>Bit</th><th>Symbol</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>TAuto</td><td colspan="2">Set to logic 1, the timer starts automatically at the end of the transmission in all communication modes at all speeds. The timer stops immediately after receiving the first data bit if the bit <i>RxMultiple</i> in the register <i>RxModeReg</i> is not set.
If <i>RxMultiple</i> is set to logic 1, the timer never stops. In this case the timer can be stopped by setting the bit <i>TStopNow</i> in register <i>ControlReg</i> to logic 1.
Set to logic 0 indicates, that the timer is not influenced by the protocol.</td></tr>
<tr><td>6 to 5</td><td>TGated</td><td colspan="2">The internal timer is running in gated mode.
Remark: In the gated mode, the bit <i>TRunning</i> is logic 1 when the timer is enabled by the register bits. This bit does not influence the gating signal.</td></tr>
<tr><td></td><td></td><td>Value</td><td>Description</td></tr>
<tr><td></td><td></td><td>00</td><td>Non gated mode</td></tr>
<tr><td></td><td></td><td>01</td><td>Gated by MFIN</td></tr>
<tr><td></td><td></td><td>10</td><td>Gated by AUX1</td></tr>
<tr><td></td><td></td><td>11</td><td>Gated by A3</td></tr>
<tr><td>4</td><td>TAutoRestart</td><td colspan="2">Set to logic 1, the timer automatically restart its count-down from <i>TReloadValue</i>, instead of counting down to zero.
Set to logic 0 the timer decrements to 0 and the bit <i>TimerIRq</i> is set to logic 1.</td></tr>
<tr><td>3 to 0</td><td>TPrescaler_Hi</td><td colspan="2">Defines higher 4 bits for <i>TPrescaler</i>.
The following formula is used to calculate f_{Timer}:
f_{Timer} = 6.78 MHz/TPreScaler.
For detailed description see Section 13 “Timer Unit”.</td></tr>
</table>

Table 93: TPrescalerReg register (address 2Bh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	TPrescaler_Hi							
Access Rights	r/w							

Table 94: Description of TPrescalerReg bits

Bit	Symbol	Description
7 to 0	TPrescaler_Lo	Defines lower 8 bits for *TPrescaler*. The following formula is used to calculate f_{Timer}: f_{Timer} = 6.78 MHz/TPreScaler. For detailed description see Section 13 “Timer Unit”.

9.2.3.11 TReloadReg

Describes the 16 bit long timer reload value.

Remark: The Reload value is split into two 8-bit registers.

Table 95: TReloadReg (Higher bits) register (address 2Ch); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Hi							
Access Rights	r/w							

Table 96: Description of higher TReloadReg bits

Bit	Symbol	Description
7 to 0	TReloadVal_Hi	Defines the higher 8 bits for the *TReloadReg*. With a start event the timer loads the *TReloadVal*. Changing this register affects the timer only at the next start event.

Table 97: TReloadReg (Lower bits)register (address 2Dh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Lo							
Access Rights	r/w							

Table 98: Description of lower TReloadReg bits

Bit	Symbol	Description
7 to 0	TReloadVal_Lo	Defines the lower 8 bits for the *TReloadReg*. With a start event the timer loads the *TReloadVal*. Changing this register affects the timer only at the next start event.

9.2.3.12 TCounterValReg

Contains the current value of the timer.

Remark: The Counter value is split into two 8-bit register.

Table 99: TCounterValReg (Higher bits) register (address 2Eh); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Hi							
Access Rights	r							

Table 100: Description of higher TCounterValReg bits

Bit	Symbol	Description
7 to 0	TCounterVal_Hi	Current value of the timer, higher 8 bits.

Table 101: TCounterValReg (Lower bits) register (address 2Fh); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Lo							
Access Rights	r							

Table 102: Description of lower TCounterValReg bits

Bit	Symbol	Description
7 to 0	TCounterVal_Lo	Current value of the timer, lower 8 bits.

9.2.4 Page 3: Test

9.2.4.1 Reserved

Functionality is reserved for further use.

Table 103: Reserved register (address 30h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFU							

Table 104: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for future use.

9.2.4.2 TestSel1Reg

General test signal configuration.

Table 105: TestSel1Reg register (address 31h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-					TstBusBitSel		
Access Rights	RFU					r/w		

Table 106: Description of TestSel1Reg bits

Bit	Symbol	Description
7 to 3	-	Reserved for future use.
2 to 0	TstBusBitSel	Select the TestBus bit from the testbus to be propagated to MFOUT.

9.2.4.3 TestSel2Reg

General test signal configuration and PRBS control

Table 107: TestSel2Reg register (address 32h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	TstBusFlip	PRBS9	PRBS15	TestBusSel				
Access Rights	r/w	r/w	r/w	r/w				

Table 108: Description of TestSel2Reg bits

Bit	Symbol	Description
7	TstBusFlip	If set to logic 1, the testbus is mapped to the parallel port by the following order: TstBusBit4,TstBusBit3, TstBusBit2,TstBusBit6,TstsBusBit5, TstBusBit0. See Section 19 “Testsignals”.
6	PRBS9	Starts and enables the PRBS9 sequence according ITU-TO150. **Remark:** All relevant registers to transmit data have to be configured before entering PRBS9 mode. The data transmission of the defined sequence is started by the send command.
5	PRBS15	Starts and enables the PRBS15 sequence according ITU-TO150. **Remark:** All relevant registers to transmit data have to be configured before entering PRBS15 mode. The data transmission of the defined sequence is started by the send command.
4 to 0	TestBusSel	Selects the testbus. See Section 19 “Testsignals”

9.2.4.4 TestPinEnReg

Enables the pin output driver on the test bus.

Table 109: TestPinEnReg register (address 33h); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	RS232LineEn	TestPinEn						-
Access Rights	r/w	r/w						RFU

Table 110: Description of TestPinEnReg bits

Bit	Symbol	Description
7	RS232LineEn	Set to logic 0, the lines MX and DTRQ for the serial UART are disabled.
6 to 1	TestPinEn	Enables the pin output driver on D1 to D7. **Example:** Setting bit 1 to logic 1 enables D1 Setting bit 5 to logic 1 enables D5 **Remark:** If the SPI interface is used only D1 to D4 can be used. If the serial UART interface is used and RS232LineEn is set to logic 1 only D1 to D4 can be used.
0	-	Reserved for future use.

9.2.4.5 TestPinValueReg

Defines the values for the test port when it is used as I/O.

Table 111: TestPinValueReg register (address 34h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	UseIO	TestPinValue						-
Access Rights	r/w	r/w						RFU

Table 112: Description of TestPinValueReg bits

Bit	Symbol	Description
7	UseIO	Set to logic 1, this bit enables the I/O functionality for the test port if one of the serial interfaces is used. The input / ouput behaviour is defined by *TestPinEn* in register *TestPinEnReg*. The value for the output behaviour is defined in the bits *TestPinVal*.
6 to 0	TestPinValue	Defines the value of the test port, when it is used as I/O. Each output has to be enabled by the *TestPinEn* bits in register *TestPinEnReg*. **Remark:** Reading the register indicates the actual status of the pins D6 - D1 if UseIO is set to logic 1. If UseIO is set to logic 0, the value of the register TestPinValueReg is read back.
0	-	Reserved for future use.

9.2.4.6 TestBusReg

Shows the status of the internal testbus.

Table 113: TestBusReg register (address 35h); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	TestBus							
Access Rights	r							

Table 114: Description of TestBusReg bits

Bit	Symbol	Description
7 to 0	TestBus	Shows the status of the internal test bus. The test bus is selected by the register *TestSel2Reg*. See Section 19 “Testsignals”.

9.2.4.7 AutoTestReg

Controls the digital selftest.

Table 115: AutoTestReg register (address 36h); reset value: 40h

Bit	7	6	5	4	3	2	1	0
Symbol	-	AmpRcv	-		SelfTest			
Access Rights	RFU	r/w	RFT		r/w			

Table 116: Description of AutoTestReg bits

Bit	Symbol	Description
7	-	Reserved for production tests.
6	AmpRcv	If set to logic 1, the internal signal processing in the receiver chain is performed non-linear. This increases the operating distance in communication modes at 106 kbit/s. **Remark:** Due to the non linearity the effect of the bits *MinLevel* and *CollLevel* in the register *RxThreshholdReg* are as well non linear.
5 to 4	-	Reserved for production tests.
3 to 0	SelfTest	Enables the digital self test. The selftest can be started by the selftest command in the command register. The selftest is enabled by 1001b. **Remark:** For default operation the selftest has to be disabled by 0000b.

9.2.4.8 VersionReg

Shows the version.

Table 117: VersionReg register (address 37h); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	Version							
Access Rights	r							

Table 118: Description of VersionReg bits

Bit	Symbol	Description
7 to 0	Version	Indicates current version. **Remark:** The current version for MFRC522 is 90h or 91h.

9.2.4.9 AnalogTestReg

Controls the pins AUX1 and AUX2

Table 119: AnalogTestReg register (address 38h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	AnalogSelAux1				AnalogSelAux2			
Access Rights	r/w				r/w			

Table 120: Description of AnalogTestReg bits

Bit	Symbol	Description	
7 to 4	AnalogSelAux1	Controls the AUX pin.	
3 to 0	AnalogSelAux2	**Remark:** All test signals are described in Section 19 “Testsignals”.	
		Value	**Description**
		0000	Tristate
		0001	Output of TestDAC1 (AUX1), output of TestDAC2 (AUX2) [1]
		0010	Testsignal Corr1 [1]
		0011	Reserved
		0100	Testsignal MinLevel [1]
		0101	Testsignal ADC channel I [1]
		0110	Testsignal ADC channel Q [1]
		0111	Reserved
		1000	Reserved, Testsignal for production test [1]
		1001	Reserved
		1010	HIGH
		1011	LOW
		1100	TxActive At 106 kbit/s: HIGH during Startbit, Databit, Parity and CRC. At 212, 424 and 848 kbit/s: High during Data and CRC.
		1101	RxActive At 106 kbit/s: High during Databit, Parity and CRC. At 212, 424 and 848 kbit/s: High during Data and CRC.
		1110	Subcarrier detected 106 kbit/s: not applicable 212, 424 and 848 kbit/s: High during last part of Data and CRC.
		1111	Test bus bit as defined by the *TstBusBitSel* in register *TestSel1Reg*.

[1] **Remark:** Current output. The use of 1 kΩ pull-down resistor on AUX is recommended

9.2.4.10 TestDAC1Reg

Defines the test values for TestDAC1.

Table 121: TestDAC1Reg register (address 39h); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	-		TestDAC1					
Access Rights	RFU		r/w					

Table 122: Description of TestDAC1Reg bits

Bit	Symbol	Description
7	-	Reserved for production tests.
6	-	Reserved for future use.
5 to 0	TestDAC1	Defines the test value for *TestDAC1*. The output of the DAC1 can be switched to AUX1 by setting *AnalogSelAux1* to 0001b in register *AnalogTestReg*.

9.2.4.11 TestDAC2Reg

Defines the test value for TestDAC2.

Table 123: TestDAC2Reg register (address 3Ah); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	-		TestDAC2					
Access Rights	RFU		r/w					

Table 124: Description ofTestDAC2Reg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5 to 0	TestDAC2	Defines the testvalue for TestDAC2. The output of the DAC2 can be switched to AUX2 by setting *AnalogSelAux2* to 0001b in register *AnalogTestReg*.

9.2.4.12 TestADCReg

Shows the actual value of ADC I and Q channel.

Table 125: TestADCReg register (address 3Bh); reset value: XXh

Bit	7	6	5	4	3	2	1	0
Symbol	ADC_I				ADC_Q			
Access Rights	r				r			

Table 126: Description of TestADCReg bits

Bit	Symbol	Description
7 to 4	ADC_I	Shows the actual value of ADC I channel.
3 to 0	ADC_Q	Shows the actual value of ADC Q channel.

9.2.4.13 Reserved

Functionality reserved for production test.

Table 127: Reserved register (address 3Ch); reset value: FFh

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFT							

Table 128: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

Table 129: Reserved register (address 3Dh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFT							

Table 130: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

Table 131: Reserved register (address 3Eh); reset value: 03h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFT							

Table 132: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

Table 133: Reserved register (address 3Fh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access Rights	RFT							

Table 134: Description of Reserved register bits

Bit	Symbol	Description
7 to 0	-	Reserved for production tests.

10. DIGITAL Interfaces

10.1 Automatic µ-Controller Interface Type Detection

The MFRC522 supports direct interfacing of various hosts as the SPI, I^2C and serial UART interface type. The MFRC522 resets its interface and checks the current host interface type automatically having performed a Power-On or Hard Reset. The MFRC522 identifies the host interface by the means of the logic levels on the control pins after the Reset Phase. This is done by a combination of fixed pin connections.The following table shows the different configurations:

Table 135: Connection Scheme for detecting the different Interface Types

MFRC522	Serial Interface Types		
Pin	**UART**	**SPI**	**I^2C**
SDA	RX	NSS	SDA
I^2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5
Remark: Overview on the pin behavior			
Pin behavior	Input	Output	In/Out

10.2 SPI Compatible interface

A serial peripheral interface (SPI compatible) is supported to enable high speed communication to the host. The SPI Interface can handle data speed of up to 10 Mbit/s. In the communication with a host MFRC522 acts as a slave receiving data from the external host for register settings and to send and receive data relevant for the communication on the RF interface.

10.2.1 General

An interface compatible to an SPI interface enables a high-speed serial communication between the MFRC522 and a µ-Controller for the communication. The implemented SPI compatible interface is according to a standard SPI interface.

For timing specification refer to Section 23.8 "Timing for the SPI compatible interface".

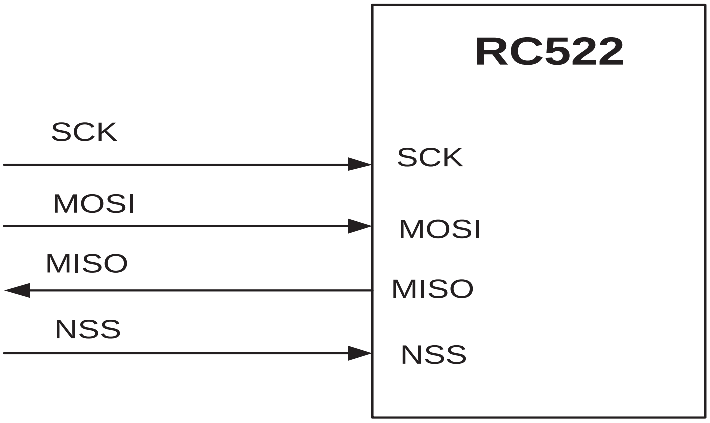


Fig 7. Connection to host with SPI

The MFRC522 acts as a slave during the SPI communication. The SPI clock SCK has to be generated by the master. Data communication from the master to the slave uses the Line MOSI. Line MISO is used to send data back from the MFRC522 to the master.

On both lines (MOSI, MISO) each data byte is sent by MSB first. Data on MOSI line should be stable on rising edge of the clock line and can changed on falling edge. The same is valid for the MISO line. Data is provided by the MFRC522 on falling edge and is stable during rising edge.

10.2.2 Read data

To read out data using the SPI compatible interface the following byte order has to be used. It is possible to read out up to n-data bytes.

The first sent byte defines both, the mode itself and the address byte.

Table 136: Byte Order for MOSI and MISO

	byte 0	byte 1	byte 2	to	byte n	byte n+1
MOSI	adr 0	adr 1	adr 2	……..	adr n	00
MISO	X	data 0	data 1	……..	data n-1	data n

Remark: The most significant bit (MSB) has to be send first.

10.2.3 Write data

To write data to the MFRC522 using the SPI interface the following byte order has to be used. It is possible to write out up to n-data bytes by only sending one's address byte.

The first send byte defines both, the mode itself and the address byte.

Table 137: Byte Order for MOSI and MISO

	byte 0	byte 1	byte 2	to	byte n	byte n+1
MOSI	adr 0	data 0	data 1	……..	data n-1	data n
MISO	X	X	X	……..	X	X

Remark: The most significant bit (MSB) has to be send first.

10.2.4 Address byte

The address byte has to fulfil the following format:

The MSB bit of the first byte defines the used mode. To read data from the MFRC522 the MSB bit is set to logic 1. To write data to the MFRC522 the MSB bit has to be set to logic 0. The bits 6 to 1 define the address and the LSB shall be set to logic 0.

Table 138. Address byte 0 register; address MOSI

7	6	5	4	3	2	1	0
1 (read) 0 (write)	address						RFU
MSB							LSB

10.3 UART Interface

10.3.1 Connection to a host

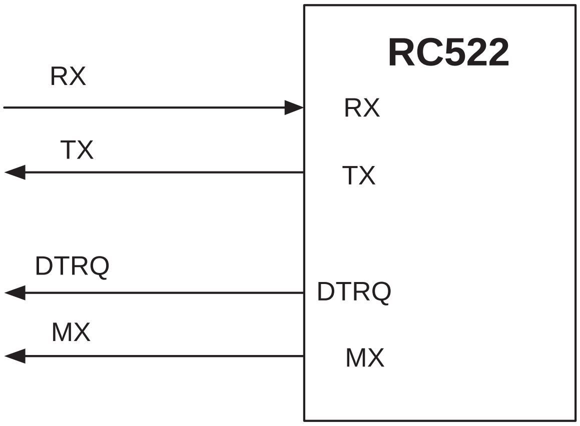


Fig 8. Connection to μ-Controllers with UART.

Remark: DTRQ and MX can be disabled by clearing the bit *RS232LineEn* in register *TestPinEnReg*.

10.3.2 Selection of the transfer speeds

The internal UART interface is compatible to an RS232 serial interface.

Table 140 “Selectable transfer speeds” describes examples for different transfer speeds and relevant register settings.

The resulting transfer speed error is less than 1.5% for all described transfer speeds.

The default transfer speed is 9.6 kbit/s.

To change the transfer speed, the host controller has to write a value for the new transfer speed to the register *SerialSpeedReg*. The bits *BR_T0* and *BR_T1* define factors to set the transfer speed in the *SerialSpeedReg*.

Table 139 “Settings of BR_T0 and BR_T1” describes the settings of *BR_T0* and *BR_T1*.

Table 139: Settings of BR_T0 and BR_T1

BR_T0	0	1	2	3	4	5	6	7
factor BR_T0	1	1	2	4	8	16	32	64
range BR_T1	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 140: Selectable transfer speeds

Transfer Speed [bit/s]	SerialSpeedReg		Transfer Speed Accuracy
	decimal	heximal	
7.2 k	250	FAh	-0.25%
9.6 k	235	EBh	0.32%
14.4 k	218	DAh	-0.25%
19.2 k	203	CBh	0.32%
38.4 k	171	ABh	0.32%
57.6 k	154	9Ah	-0.25%
115.2 k	122	7Ah	-0.25%
128 k	116	74h	-0.06%
230.4 k	90	5Ah	-0.25%
460.8 k	58	3Ah	-0.25%
921.6 k	28	1Ch	1.45%
1228.8 k	21	15h	0.32%

The selectable transfer speeds as shown in Table 140 “Selectable transfer speeds” are calculated according to the following formulas:

if $BR\_T0=0$: transfer speed = 27.12 MHz/(BR_T1+1)

if $BR\_T0>0$: transfer speed = 27.12 MHz/(BR_T1 +33)/2^(BR_T0 -1)

Remark: Transfer speeds above 1228.8 k are not supported.

10.3.3 Framing

Table 141: UART Framing

	Length	Value
Start bit	1 bit	0
Data bits	8 bits	Data
Stop bit	1 bit	1

Remark: For data and address bytes the LSB bit has to be sent first.
No parity bit is used during transmission.

Read data:

To read out data using the UART interface the flow described below has to be used. The first send byte defines both the mode itself and the address.

Table 142: Byte Order to Read Data

	byte 0	byte 1
RX	adr	
TX		data 0

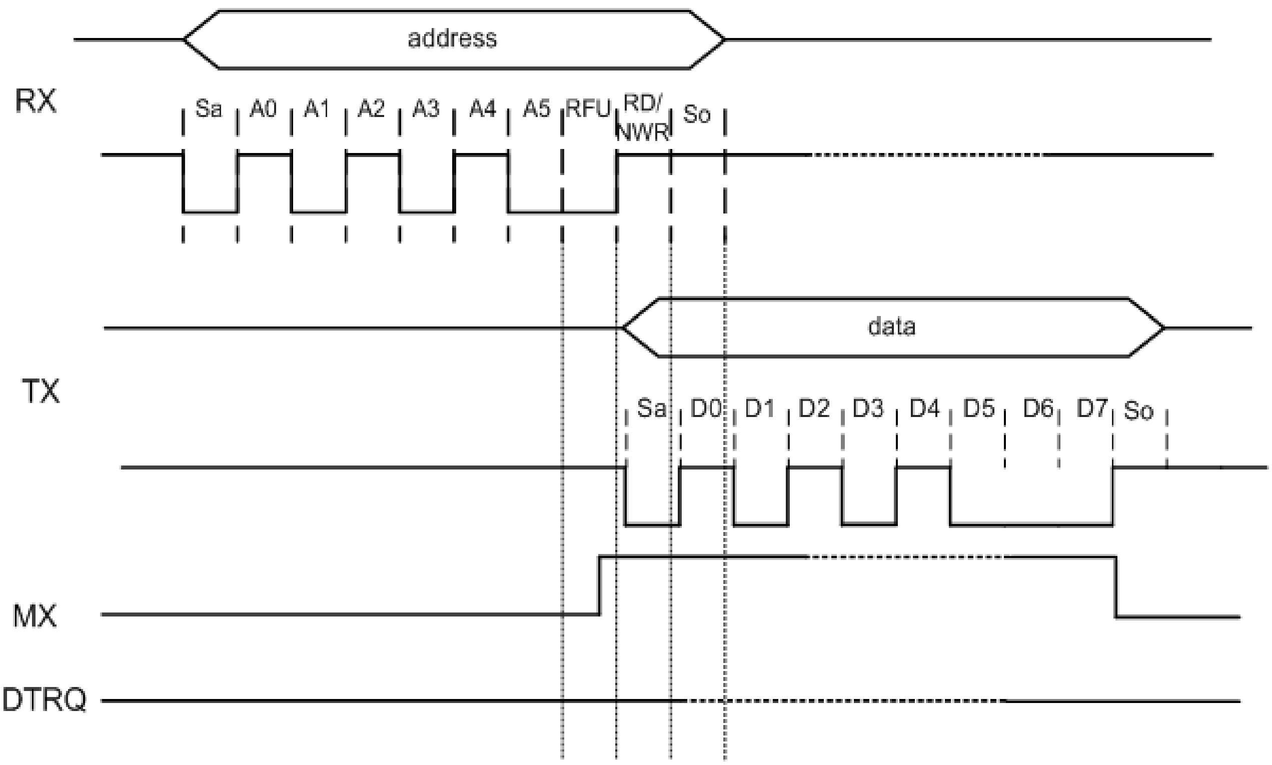


Fig 9. Schematic Diagram to Read Data

Write data:

To write data to the MFRC522 using the UART interface the following structure has to be used.

The first send byte defines both, the mode itself and the address.

Table 143: Byte Order to Write Data

	byte 0	byte 1
RX	adr 0	data 0
TX		adr 0

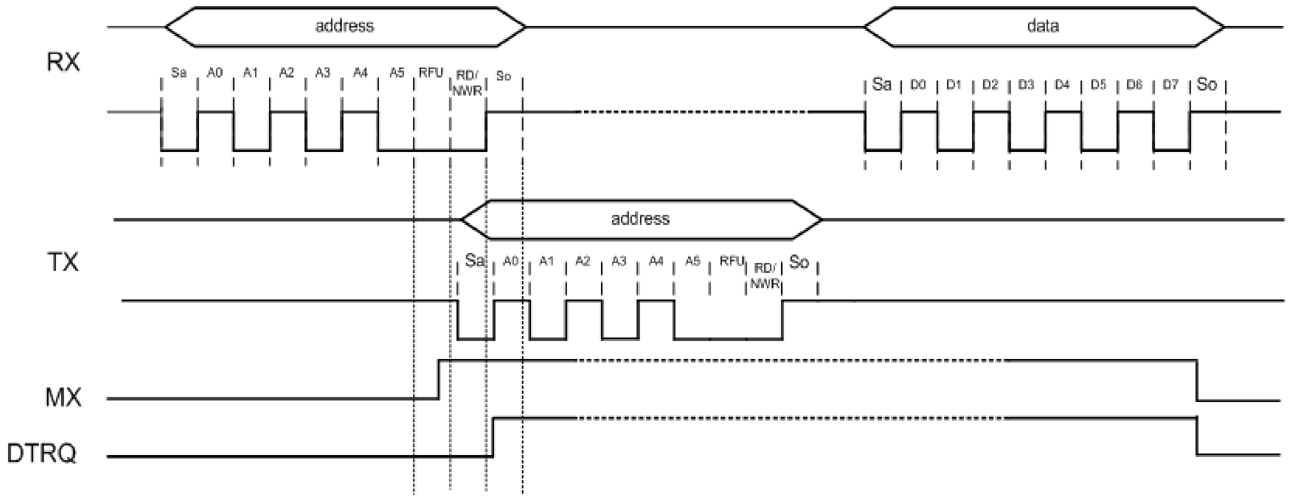


Fig 10. Schematic Diagram to Write Data.

Remark: The data byte can be send directly after the address byte on RX.

Address byte:

The address byte has to fulfil the following format:

The MSB of the first byte sets the used mode. To read data from the MFRC522 the MSB is set to logic 1. To write data to the MFRC522 the MSB has to be set to logic 0. The bit 6 is reserved for further use and the bits 5 to 0 define the address.

Table 144. Address byte 0 register; address MOSI

7	6	5	4	3	2	1	0
1 (read) 0 (write)	RFU	address					
MSB							LSB

10.4 I^{2}C Bus Interface

An Inter IC (I^{2}C) bus interface is supported to enable a low cost, low pin count serial bus interface to the host. The implemented I^{2}C interface is implemented according the NXP Semiconductors I^{2}C interface specification, rev. 2.1, January 2000. The implemented interface can only act in Slave mode. Therefore no clock generation and access arbitration is implemented in the MFRC522.

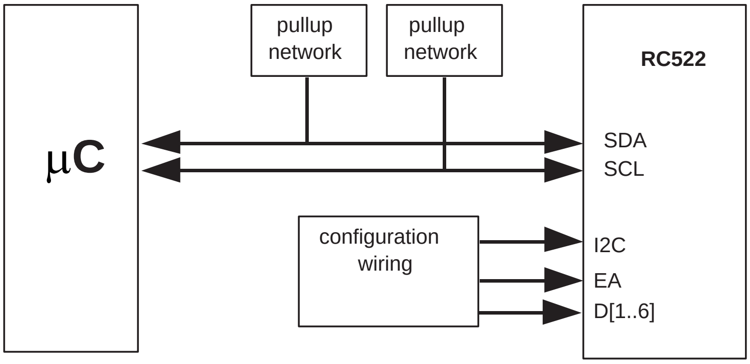


Fig 11. I^{2}C interface.

10.4.1 General

The implemented interface is conform to the I^{2}C-bus specification version 2.1, January 2000. The MFRC522 can act as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bi-directional line, connected to a positive supply voltage via a current-source or a pull-up resistor. Both lines SDA and SCL are set to HIGH level if no data is transmitted. The MFRC522 has a tri-state output stage to perform the wired-AND function. Data on the I^{2}C-bus can be transferred at data rates of up to 100 kbit/s in Standard mode, up to 400 kbit/s in the Fast mode or up to 3.4 Mbit/s in the High-speed mode.

If the I^{2}C interface is selected, a spike suppression according to the I^{2}C interface specification on SCL and SDA is activated.

For timing requirements refer to Section 23.9 “I^{2}C Timing”

10.4.2 Data validity

Data on the SDA line shall be stable during the HIGH period of the clock. The HIGH or LOW state of the data line shall only change when the clock signal on SCL is LOW.

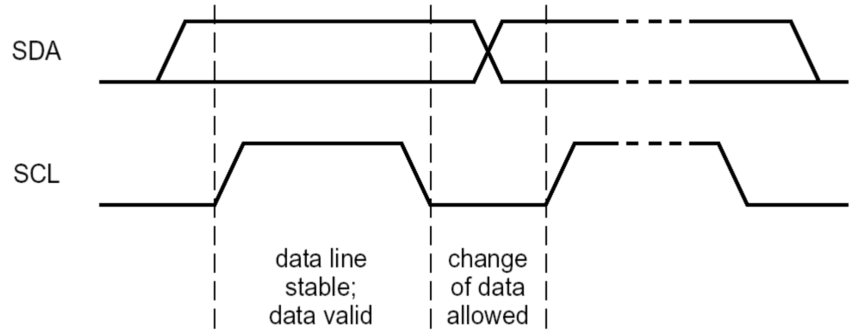


Fig 12. Bit transfer on the I²C-bus.

10.4.3 START and STOP conditions

To handle the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

A START condition is defined with a HIGH to LOW transition on the SDA line while SCL is HIGH.

A STOP condition is defined with a LOW to HIGH transition on the SDA line while SCL is HIGH.

The master always generates the START and STOP conditions. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical. Therefore, the S symbol will be used as a generic term to represent both the START and repeated START (Sr) conditions.

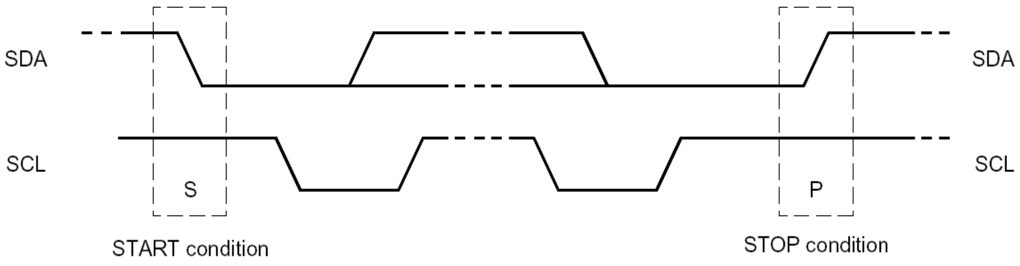


Fig 13. START and STOP conditions.

10.4.4 Byte format

Each byte has to be followed by an acknowledge bit. Data is transferred with the MSB first, see Figure 16 “First byte following the START procedure.”. The number of transmitted bytes during one data transfer is unrestricted but shall fulfil the read/ write cycle format.

10.4.5 Acknowledge

An acknowledge at the end of one data byte is mandatory. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver shall pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer, or a repeated START (Sr) condition to start a new transfer.

A master-receiver shall indicate the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter shall release the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

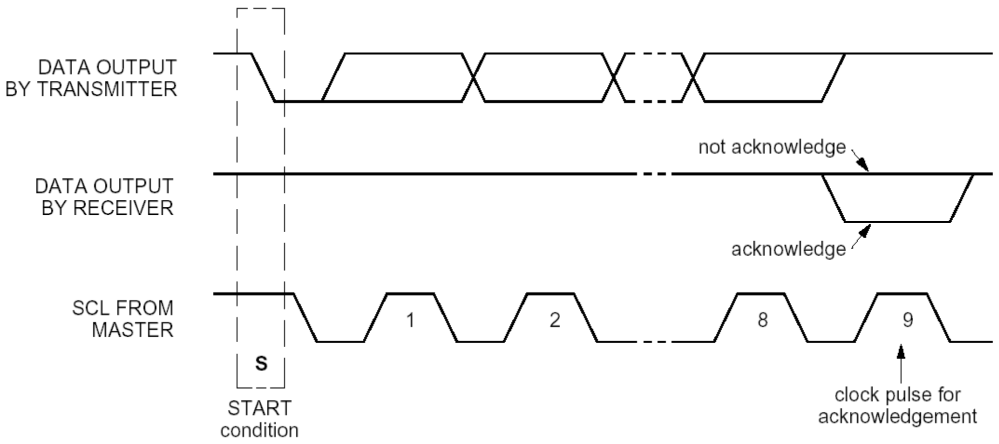


Fig 14. Acknowledge on the I^{2}C- bus.

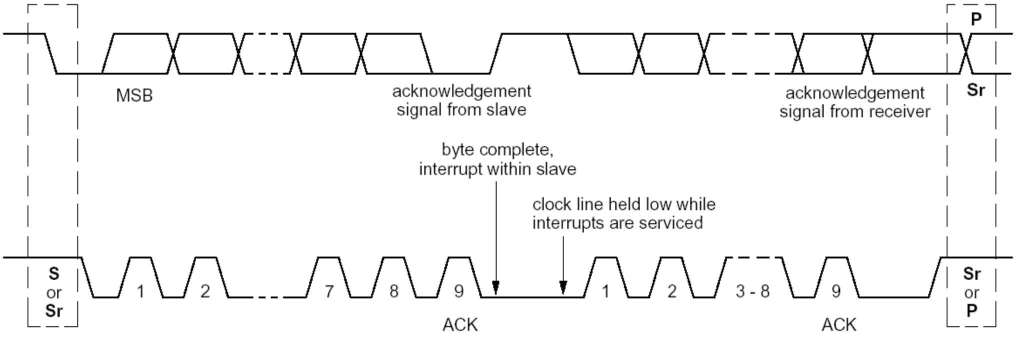


Fig 15. Data transfer on the I2C- bus.

10.4.6 7-BIT ADDRESSING

During the I2C-bus addressing procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

As an exception several address numbers are reserved. During device configuration, the designer has to ensure, that no collision with these reserved addresses is possible. Check the corresponding I2C specification for a complete list of reserved addresses.

The I2C address specification is dependent on the definition of the EA Pin. Immediately after releasing the reset pin or after power on reset, the device defines the I2C address according EA pin.

If EA Pin is set to LOW than for all MFRC522 devices the upper 4 bits of the device bus address are reserved by NXP and set to 0101(bin). The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the Slave Address can freely configured by the customer in order to prevent collisions with other I2C devices.

If EA Pin is set to HIGH than ADR_0 to ADR_5 can be completely specified at the external pins according to Table Table 135 “Connection Scheme for detecting the different Interface Types”. ADR_6 is always set to logic 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I2C address pins could be used for test signal output.

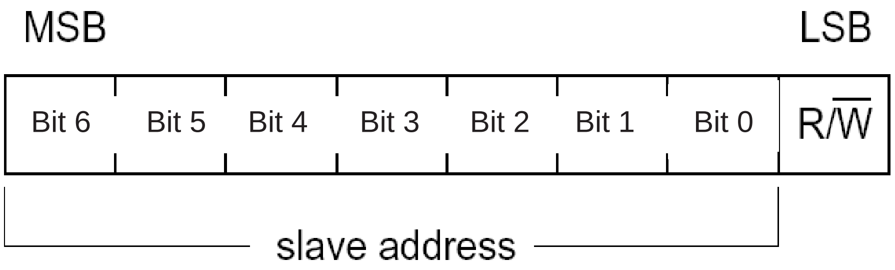


Fig 16. First byte following the START procedure.

10.4.7 Register Write Access

To write data from the host controller via I^{2}C to a specific register of the MFRC522 the following frame format shall be used.

The first byte of a frame indicates the device address according to the I^{2}C rules. The second byte indicates the register address followed by up to n-data bytes. In one frame all n-data bytes are written to the same register address. This enables for example a fast FIFO access.

The read/write bit shall be set to logic 0.

10.4.8 Register Read Access

To read out data from a specific register address of the MFRC522 the host controller shall use the procedure:

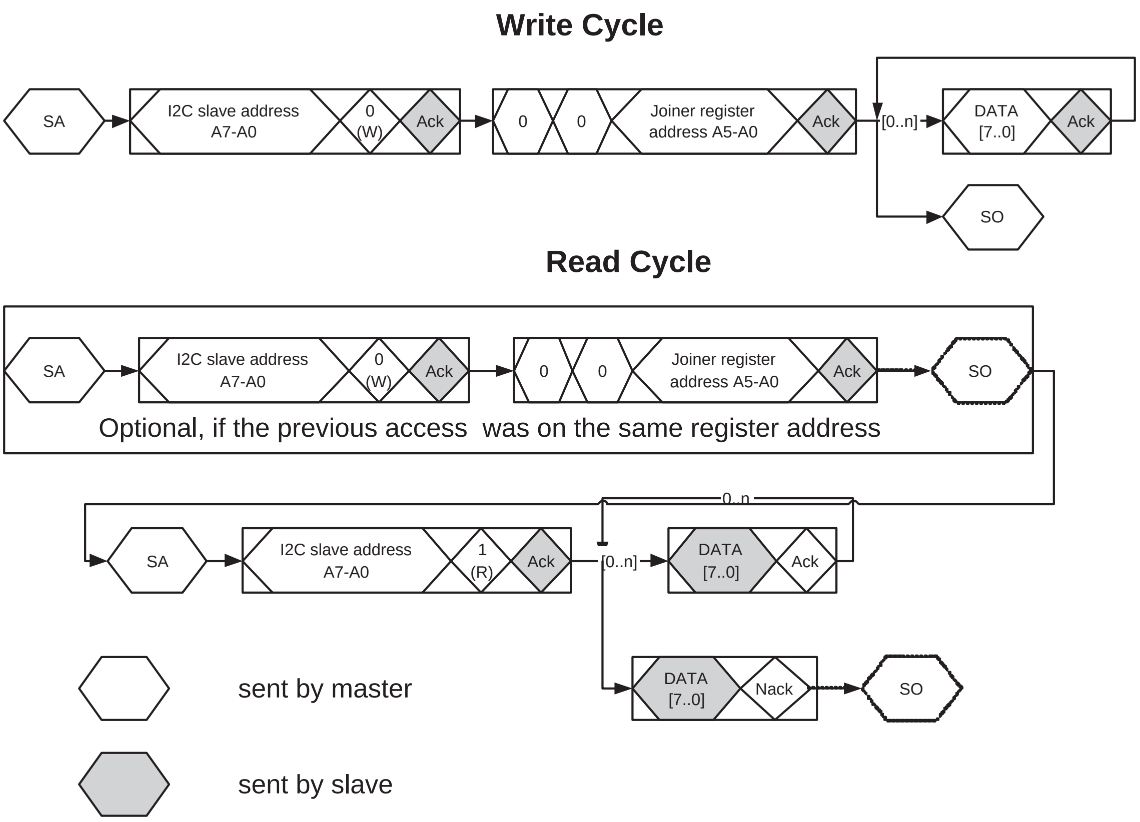
First a write access to the specific register address has to be performed as indicated in the following frame.

The first byte of a frame indicates the device address according to the I^{2}C rules. The second byte indicates the register address. No data bytes are added.

The read/write bit shall be 0.

Having performed this write access, the read access can start. The host has to send the device address of the MFRC522. As an answer to this the MFRC522 responds with the content of this register. In one frame all n-data bytes could be read from the same register address. This enables for example a fast FIFO access or register polling.

The read/write bit shall be set to logic 1.



SA	start condition
SO	stop condition
ACK	acknowledge
Nack	not acknowlege
(W)	write cycle
(R)	read cycle

Fig 17. Register Read and Write Access

10.4.9 HS mode

In High-speed mode (HS mode) the device can transfer information at data rates of up to 3.4 Mbit/s, it remains fully downward compatible with Fast- or Standard mode (F/S mode) for bi-directional communication in a mixed-speed bus system.

10.4.10 High Speed Transfer

To achieve a data rates of up to 3.4 Mbit/s the following improvements have been made to the regular I^{2}C-bus behavior.

- The inputs of the device in HS mode incorporates spike suppression and a Schmitt-trigger at the SDA and SCL inputs with different timing constants compared to F/S mode.
- The output buffers of the device in HS mode incorporates slope control of the falling edges of the SDA and SCL signals with different fall time compared to F/S mode.

10.4.11 Serial Data transfer Format in HS mode

Serial data transfer format in HS mode meets the Standard mode I^{2}C-bus specification. HS mode can only commence after the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001XXX)
3. Not-acknowledge bit (A)

The active master then sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address, and receives an acknowledge bit (A) from the selected MFRC522.

Data transfer continues in in Hs-mode after the next repeated START (Sr), and only switches back to F/S-mode after a STOP condition (P). To reduce the overhead of the master code, it's possible that a master links a number of Hs-mode transfers, separated by repeated START conditions (Sr).

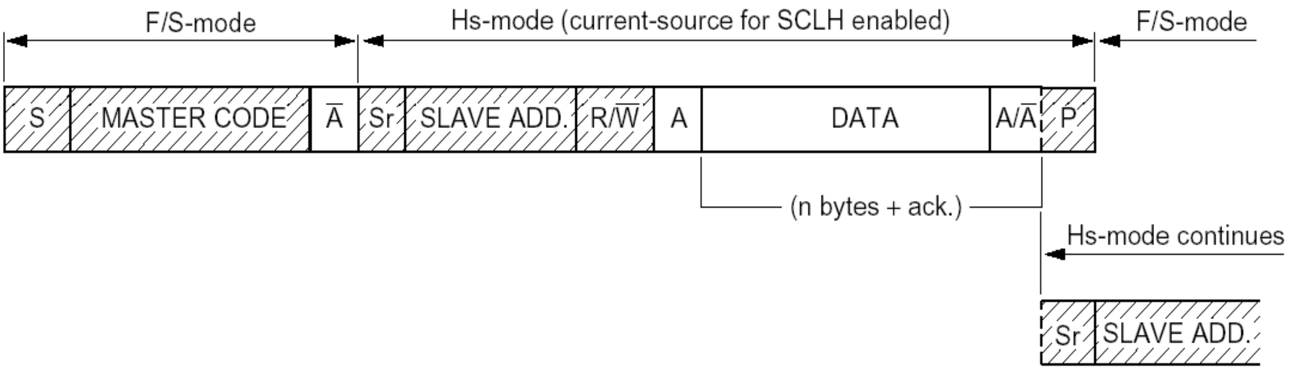


Fig 18. I^{2}C HS mode protocol switch

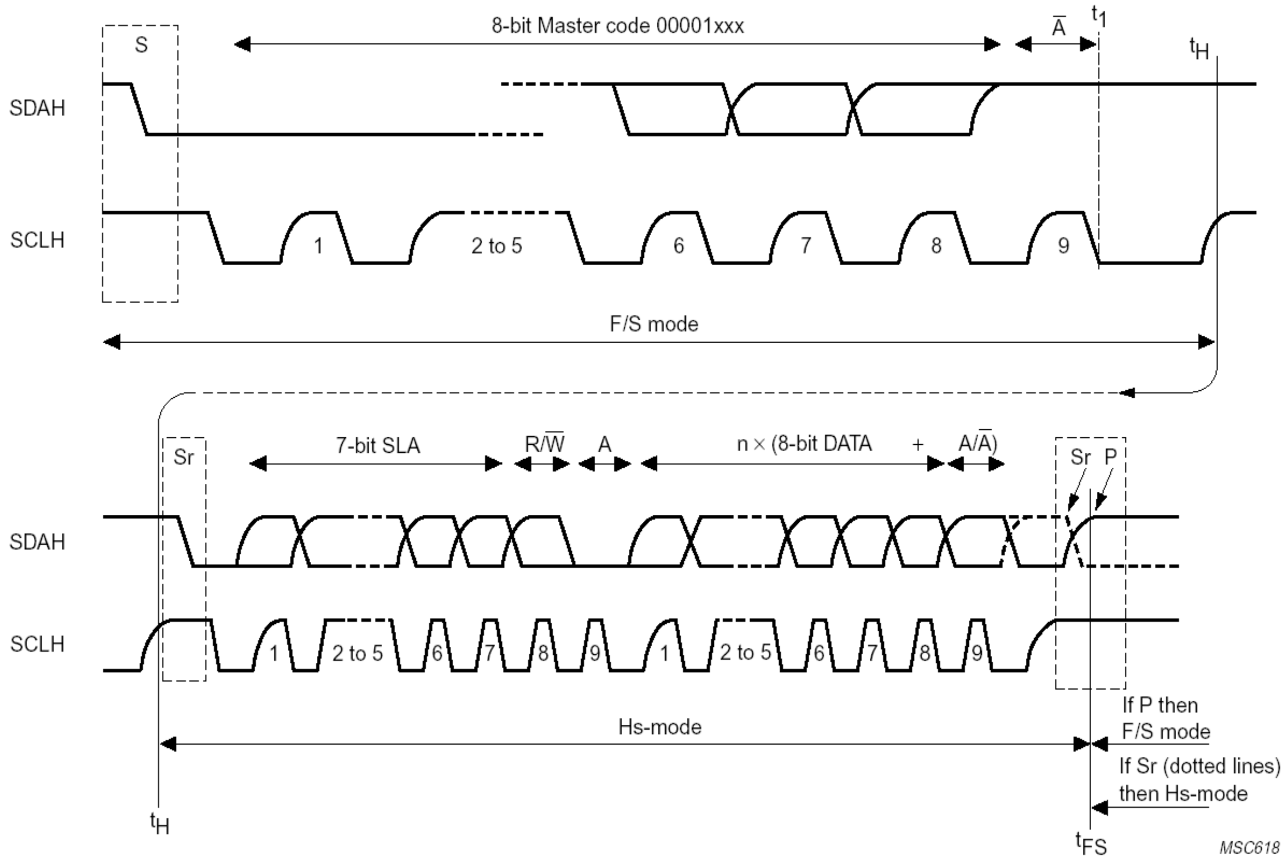


Fig 19. I²C HS mode protocol frame

10.4.12 Switching from F/S to HS mode and Vice Versa

After reset and initialization, the MFRC522 is in Fast mode (which is in effect F/S mode as Fast mode is downward compatible to Standard mode). The connected MFRC522 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

Following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

For system configurations, where no other I^2C devices are involved in the communication, have an additional possibility to switch to HS-mode. By setting the bit *I*^{2}*CForceHS* in register *Status2Reg* to logic 1, the HS mode is entered. Setting this bit to logic 1 changes the HS-mode permanent meaning that sending the master code is no longer necessary. This is not according the specification and should only be used when no other devices are connected on the bus. Spikes on the I^2C lines shall be avoided because of the reduced spike suppression.

10.4.13 MFRC522 at Lower Speed modes

MFRC522 is fully downwards compatible, and can be connected to an F/S mode I^2C-bus system. As no master code will be transmitted in such a configuration, the device stays in F/S mode and communicates at F/S mode speeds.

11. Analog Interface and Contactless UART

11.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kbit/s. An external circuit can to be connected to the communication interface pins MFIN/MFOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication schemes in co-operation with the host. The protocol handling itself generates bit- and byte-oriented framing and handles error detection like Parity and CRC according to the different contactless communication schemes.

Remark: The size and the tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

11.2 TX Driver

The signal delivered on pin TX1 and pin TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly, using a few passive components for matching and filtering, see Section 24 “Application information”. The signal on TX1 and TX2 can be configured by the register *TxControlReg*, see Section 9.2.2.5 “TxControlReg”.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured by the registers *CWGsPReg* and *ModGsPReg*. The impedance of the n-driver can be configured by the register *GsNReg*. Furthermore, the modulation index depends on the antenna design and tuning.

The register *TxModeReg* and *TxAutoSelReg* control the data rate and framing during transmission and the setting of the antenna driver to support the different requirements at the different modes and transfer speeds.

Table 145: Settings for TX1

TX1RFEn	Force 100ASK	InVTx1 RFON	InVTx1 RFOFF	Envelope	TX1	GSPMos	GSNMos	Remarks
0	X	x	x	x	x	x	x	not specified if RF is switched off
1	0	0	x	0	RF	pMod	nMod	100% ASK: TX1 pulled to 0, independent of *InvTx1RFOff*
				1	RF	pCW	nCW	
	0	1	X	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	x	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

Table 146: Settings for TX2

TX1RFEn	Force 100ASK	TX2CW	InVTx2 RFON	InVTx2 RFOFF	Envelope	TX2	GSPMos	GSNMos	Remarks
0	x	x	x	x	x	x	x	x	not specified if RF is switched off
1	0	0	0	x	0	RF	pMod	nMod	
					1	RF	pCW	nCW	
			1	X	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	x	X	RF	pCW	nCW	Gs always CW for TX2CW
			1	x	X	RF_n	pCW	nCW	
	1	0	0	x	0	0	pMod	nMod	100%ASK:Tx2 pulled to 0 (independent of *InvTx2RFOn*/*INVTX2RFOff*)
					1	RF	pCW	nCW	
			1	x	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	x	X	RF	pCW	nCW	
			1	x	X	RF_n	pCW	nCW	

The following abbreviations are used:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz divided by 2
- RF_n: inverted 13.56 MHz clock
- gspmos: Conductance, configuration of the PMOS array
- gspmos: Conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuos wave defined by *CWGsP* register
- pMod: PMOS conductance value for modulation defined by *ModGsP* register
- nCW: NMOS conductance value for continuos wave defined by *CWGsN* register
- nMod: NMOS conductance value for modulation defined by *ModGsN* register

Remark: If only 1 driver is switched on, the values for *ModGsN*, *ModGsP* and *CWGsN*, *CWGsP* are used for both drivers.

11.3 Serial Data Switch

Two main blocks are implemented in the MFRC522. A digital circuitry, comprising state machines, coder and decoder logic and an analog circuitry with the modulator and antenna drivers, receiver and amplification circuitry. For example, the interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins MFIN and MFOUT.

This topology supports, that the analog part of the MFRC522 may be connected to the digital part of another device.

The serial signal switch is controlled by the register *TxSelReg* and *RxSelReg*.

The following figure shows the serial data switch for TX1 and TX2.

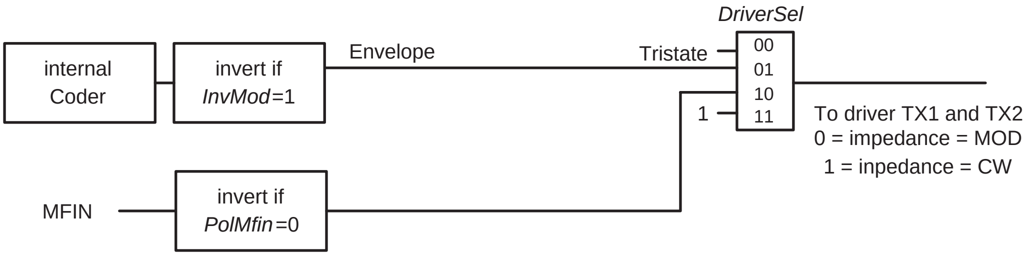


Fig 20. Serial data switch for TX1 and TX2.

11.4 MFIN/MFOUT interface support

The MFRC522 is basically divided into digital circuitry and analog circuitry. The digital circuitry contains state machines, coder and decoder logic and so on and the analog circuitry contains the modulator and antenna drivers, receiver and amplification circuitry. The interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins MFIN and MFOUT (see Figure 21 “Overview MFIN/MFOUT Signal Routing”). The configuration is done by bits *MFOutSel*, *DriverSel* and *UARTSel* of registers *TxSelReg* and *RxSelReg*.

This topology supports, that some parts of the analog part of the MFRC522 may be connected to the digital part of another device.

The switch *MFOutSel* in register *TxSelReg* can be used to measure MIFARE® and ISO/IEC14443 related signals. This is especially important during the design In phase or for test purposes to check the transmitted and received data.

However, the most important use of MFIN/MFOUT pins is the active antenna concept. An external active antenna circuit can be connected to the digital circuit of the MFRC522. *MFOutSel* has to be configured in that way that the signal of the internal Miller Coder is send to MFOUT pin (*MFOutSel* = 4). *UARTSel* has to be configured to receive Manchester signal with sub-carrier from MFIN pin (*UARTSel* = 1).

It is possible, to connect a 'passive antenna' to pins TX1, TX2 and RX (via the appropriate filter and matching circuit) and at the same time an Active Antenna to the pins MFOUT and MFIN. In this configuration, two RF-parts may be driven (one after another) by one host processor.

Remark: The MFRC522 has an extra supply pin (SVDD and PVSS as Ground line) for the MFIN and MFOUT pads.
If MFIN pin is not used it should be connected to SVDD or PVSS.
If SVDD pin is not used it should be connected to DVDD or PVDD or any other voltage supply pin.

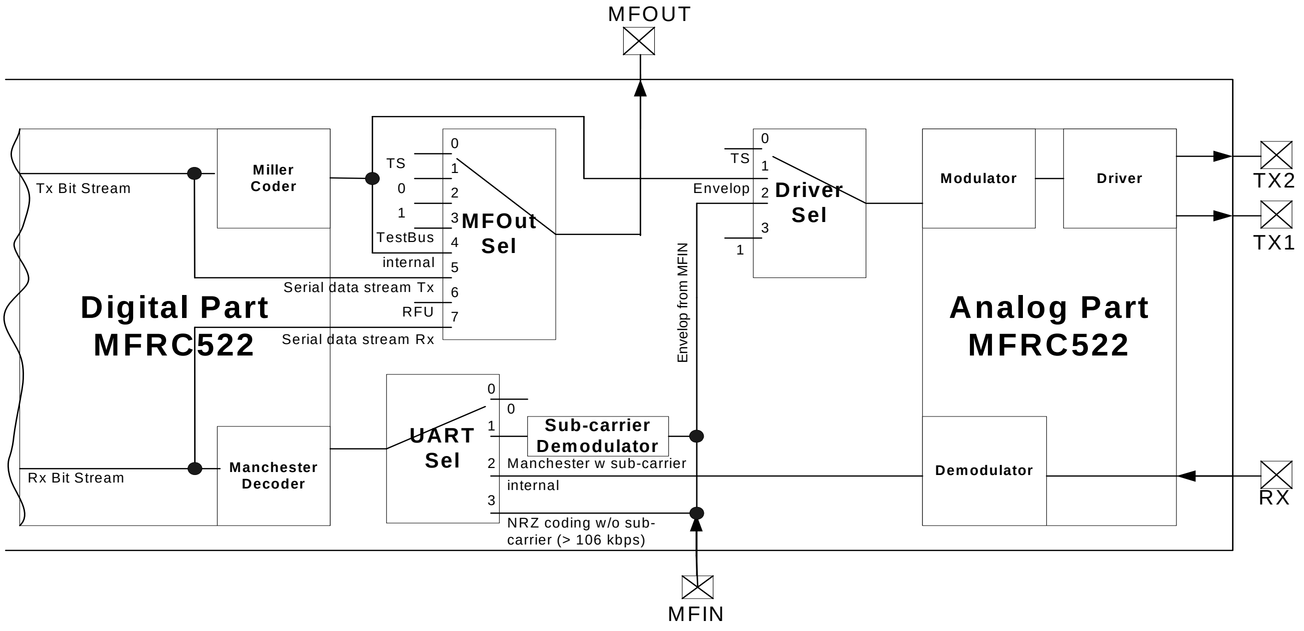


Fig 21. Overview MFIN/MFOUT Signal Routing

11.5 CRC co-processor

The following parameters of the CRC co-processor can be configured. The CRC preset value can either be 0000h, 6363h, A671h or FFFFh depending on the bits CRCPreset in register *ModeReg*.

The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$.

The register *CRCResultReg* indicates the result of the CRC calculation. This register is split into two 8-bit registers indicating the higher and lower byte.

The bit *MSBFirst* in the register *ModeReg* indicates that data will be loaded with MSB first.

Table 147: CRC co-processor parameters

Parameter	Value
CRC Register Length	16 bit CRC
CRC Algorithm	Algorithm according ISO/IEC 14443A and CCITT
CRC Preset Value	0000h, 6363h,A671h or FFFFh depending on the *CRCPresetReg* register settings

12. FIFO Buffer

12.1 Overview

An 64 × 8-bit FIFO buffer is implemented in the MFRC522. It buffers the input and output data stream between the host and the internal state machine of the MFRC522. Thus, it is possible to handle data streams with lengths of up to 64 bytes without taking timing constraints into account.

12.2 Accessing the FIFO Buffer

The FIFO-buffer input and output data bus is connected to the register *FIFODataReg*. Writing to this register stores one byte in the FIFO-buffer and increments the internal FIFO-buffer write-pointer. Reading from this register shows the FIFO-buffer contents stored at the FIFO-buffer read-pointer and decrements the FIFO-buffer read-pointer. The distance between the write- and read-pointer can be obtained by reading the register *FIFOLevelReg*.

When the μ-Controller starts a command, the MFRC522 may, while the command is in progress, access the FIFO-buffer according to that command. Physically only one FIFO-buffer is implemented, which can be used in input- and output direction. Therefore the μ-Controller has to take care, not to access the FIFO-buffer in an unintended way.

12.3 Controlling the FIFO-Buffer

Besides writing to and reading from the FIFO-buffer, the FIFO-buffer pointers might be reset by setting the bit *FlushBuffer* in the register *FIFOLevelReg* to 1. Consequently, the *FIFOLevel* bits are set to logic 0, the bit *BufferOvfl* in the register *ErrorReg* is cleared, the actually stored bytes are not accessible any more and the FIFO-buffer can be filled with another 64 bytes again.

12.4 Status Information about the FIFO-Buffer

The host may obtain the following data about the FIFO-buffers status:

- Number of bytes already stored in the FIFO-buffer: *FIFOLevel* in register *FIFOLevelReg*
- Warning, that the FIFO-buffer is almost full: *HiAlert* in register *Status1Reg*
- Warning, that the FIFO-buffer is almost empty: *LoAlert* in register *Status1Reg*
- Indication, that bytes were written to the FIFO-buffer although it was already full: *BufferOvfl* in register *ErrorReg*. *BufferOvfl* can be cleared only by setting bit *FlushBuffer* in the register *FIFOLevelReg*.

The MFRC522 can generate an interrupt signal

- If *LoAlertIEn* in register *CommIEnReg* is set to logic 1 it will activate pin IRQ when *LoAlert* in the register *Status1Reg* changes to 1.
- If *HiAlertIEN* in register *CommIEnReg* is set to logic 1 it will activate pin IRQ when *HiAlert* in the register *Status1Reg* changes to 1.

The bit *HiAlert* is set to logic 1 if maximum *WaterLevel* bytes (as set in register *WaterLevelReg*) or less can be stored in the FIFO-buffer. It is generated according to the following equation:

$$HiAlert = (64 - FIFOLength) \leq WaterLevel$$

The bit *LoAlert* is set to logic 1 if *WaterLevel* bytes (as set in register *WaterLevelReg*) or less are actually stored in the FIFO-buffer. It is generated according to the following equation:

$$LoAlert = FIFOLength \leq WaterLevel$$

13. Timer Unit

A timer unit is implemented in the MFRC522. The external host may use this timer to manage timing relevant tasks. The timer unit may be used in one of the following configurations:

- Time-out counter
- Watch-dog counter
- Stop watch
- Programmable one-shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events which will be explained in the following, but the timer itself does not influence any internal event (e.g. A time-out during data reception does not influence the reception process automatically). Furthermore, several timer related bits are set and these bits can be used to generate an interrupt.

The timer has an input clock of 6.78 MHz (derived from the 27.12 MHz quartz). The timer consists of two stages: 1 prescaler and 1 counter.

The prescaler is a 12 bit counter. The reload value for TPrescaler can be defined between 0 and 4095 in register *TModeReg* and *TPrescalerReg*.

The reload value for the counter is defined by 16 bits in a range of 0 to 65535 in the register *TReloadReg*.

The current value of the timer is indicated by the register *TCounterValReg*.

If the counter reaches 0 an interrupt will be generated automatically indicated by setting the *TimerIRq* bit in the register *CommonIRqReg*. If enabled, this event can be indicated on the IRQ line. The bit *TimerIRq* can be set and reset by the host. Depending on the configuration the timer will stop at 0 or restart with the value in register *TReloadReg*.

The status of the timer is indicated by bit *TRunning* in register *Status1Reg*.

The timer can be manually started by *TStartNow* in register *ControlReg* or manually stopped by *TStopNow* in register *ControlReg*.

Furthermore the timer can be activated automatically by setting the bit *TAuto* in the register *TModeReg* to fulfil dedicated protocol requirements automatically.

The time delay of a timer stage is the reload value +1.

Maximum time: TPrescaler = 4095, TReloadVal = 65535
=> 4096 × 65536/6.78 MHz = 39.59 s

Example:

> To indicate 100 us it is required to count 678 clock cycles. This means the value for TPrescaler has to be set to TPrescaler = 677.The timer has now an input clock of 100 us. The timer can count up to 65535 timeslots of each 100 us.

14. Interrupt Request System

The MFRC522 indicates certain events by setting bit *IRq* in the register *Status1Reg* and additionally, if activated, by pin IRQ. The signal on pin IRQ may be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

The following table shows the available interrupt bits, the corresponding source and the condition for its activation. The interrupt bit *TimerIRq* in register *CommIRqReg* indicates an interrupt set by the timer unit. The setting is done when the timer decrements from 1 down to 0.

The *TxIRq* bit in register *CommIRqReg* indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit sets the interrupt bit automatically. The CRC coprocessor sets the bit *CRCIRq* in the register *DivIRqReg* after having processed all data from the FIFO buffer. This is indicated by the bit *CRCReady* = 1.

The bit *RxIRq* in register *CommIRqReg* indicates an interrupt when the end of the received data is detected.

The bit *IdleIRq* in register *CommIRqReg* is set if a command finishes and the content of the command register changes to idle.

The bit *HiAlertIRq* in register *CommIRqReg* is set to logic 1 if the *HiAlert* bit is set to logic 1, that means the FIFO buffer has reached the level indicated by the bit *WaterLevel*.

The bit *LoAlertIRq* in register *CommIRqReg* is set to logic 1 if the *LoAlert* bit is set to logic 1, that means the FIFO buffer has reached the level indicated by the bit *WaterLevel*.

The bit *ErrIRq* in register *CommIRqReg* indicates an error detected by the contactless UART during sending or receiving. This is indicated by any bit set to logic 1 in register *ErrorReg*.

Table 148: Interrupt Sources

Interrupt bit	Interrupt Source	Is set automatically, when
TimerIRq	Timer Unit	the timer counts from 1 to 0
TxIRq	Transmitter	a transmitted data stream ends
CRCIRq	CRC co-processor	all data from the FIFO buffer has been processed
RxIRq	Receiver	a received data stream ends
IdleIRq	Command Register	a command execution finishes
HiAlertIRq	FIFO-buffer	the FIFO-buffer is getting full
LoAlertIRq	FIFO-buffer	the FIFO-buffer is getting empty
ErrIRq	contactless UART	an error is detected

15. Oscillator Circuitry

The clock applied to the MFRC522 acts as time basis for the coder and decoder of the synchronous system. Therefore stability of the clock frequency is an important factor for proper performance. To obtain highest performance, clock jitter has to be as small as possible. This is best achieved by using the internal oscillator buffer with the recommended circuitry. If an external clock source is used, the clock signal has to be applied to pin OSCIN. In this case special care for clock duty cycle and clock jitter is needed and the clock quality has to be verified.

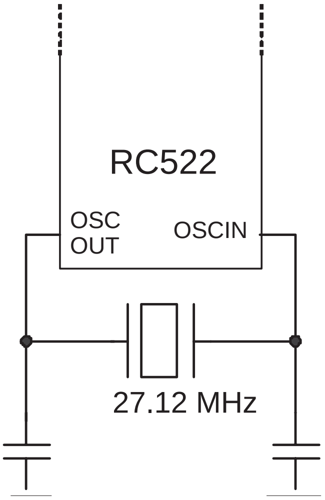


Fig 22. Ouartz Connection

16. Power Reduction modes

16.1 Hard Power-down

A Hard Power-down is enabled with LOW level on pin NRSTPD. This turns off all internal current sinks as well as the oscillator. All digital input buffers are separated from the input pads and clamped internally (except pin NRSTPD itself). The output pins are frozen at a certain value.

16.2 Soft Power-down

The Soft Power-down mode is entered immediately after setting the bit *PowerDown* in the register *CommandReg* to 1. All internal current sinks are switched off (including the oscillator buffer).

In opposition to the Hard Power-down mode, the digital input-buffers are not separated by the input pads and keep their functionality. The digital output pins do not change their state.

During Soft Power-down, all registers values, the FIFO’s content and the configuration itself will keep its current content.

After setting bit *PowerDown* in the register *CommandReg* to 0 it takes 1024 clocks until the Soft Power-down mode is left as indicated by the *PoweDown* bit itself. Setting it to logic 0 does not immediately clear it. It is cleared automatically by the MFRC522 when the Soft Power-down mode is left.

Remark: If the internal oscillator is used, you have to take into account that it is supplied by AVDD and it will take a certain time t_{osc} until the oscillator is stable and the clock cycles can be detected by the internal logic.
For the serial UART it is recommended to send the value 55 (hex) to the MFRC522 first. For further access to the registers the oscillator must be stable. Therefore, perform a read accesses to address 0 till the MFRC522 answers to the last read command with the register content of address 0. This indicates that the MFRC522 is active for further operation.

16.3 Transmitter Power-down

The Transmitter Power-down mode switches off the internal antenna drivers to turn off the RF field by setting either *Tx1RfEn* or *TX2RFEn* in the register *TXControlReg* to logic 0.

17. Reset and Oscillator Startup Time

17.1 Reset Timing Requirements

The reset signal is filtered by a hysteresis circuit and a spike filter (rejects signals shorter than 10 ns) before it enters the digital circuit. In order to perform a reset, the signal has to be low for at least 100 ns.

17.2 Oscillator Startup Time

Having set the MFRC522 to a Power-down mode or supplying the IC with XVDD the following figure describes the startup timing for the oscillator.

The time $t_{startup}$ defines the startup time of crystal oscillator circuit. The crystal oscillator startup time is defined by the crystal itself.

The t_{delay} defines the internal delay time of the MFRC522 when the clock signal is stable before the MFRC522 can be addressed. The delay time is calculated as follows:
t_{delay} [µs] = 1024/27.12 = 37.76 µs.

The time t_{osc} is defined as the sum of the time t_{delay} and $t_{startup}$.

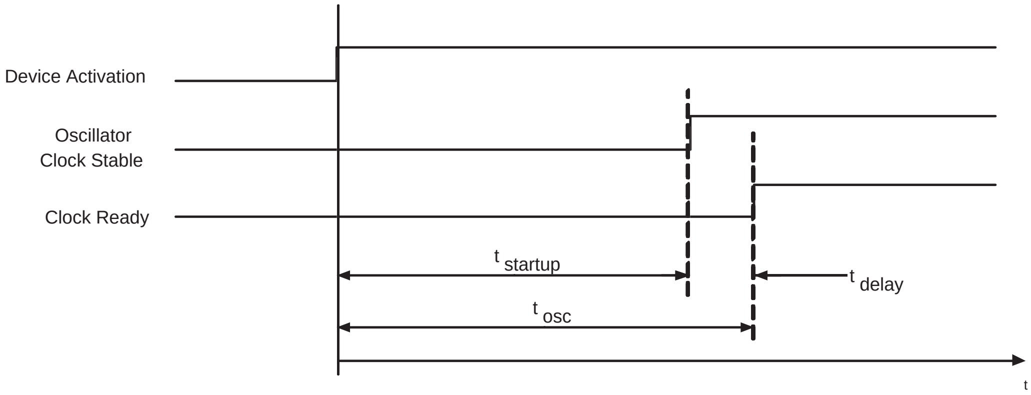


Fig 23. Oscillator Startup time.

18. MFRC522 Command Set

18.1 General Description

The behavior is determined by a state machine capable to perform a certain set of commands. By writing the according command-code to register *CommandReg* the command is executed.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

18.2 General Behavior

- Each command, that needs a data stream (or data byte stream) as input will immediately process the data it finds in the FIFO buffer. An exception to this rule is the Transceive command. Using this command the transmission is started with the *StartSend* bit in the *BitFramingReg* register.
- Each command that needs a certain number of arguments will start processing only when it has received the correct number of arguments via the FIFO buffer.
- The FIFO buffer is not cleared automatically at command start. Therefore, it is also possible to write the command arguments and/or the data bytes into the FIFO buffer and start the command afterwards.
- Each command may be interrupted by the host by writing a new command code into register *CommandReg* e.g.: the Idle-Command.

18.3 MFRC522 Commands Overview

Table 149: Command overview

Command	Command code	Action
Idle	0000	No action; cancels current command execution.
Mem	0001	Stores 25 byte into the internal buffer
Generate RandomID	0010	Generates a 10 byte random ID number
CalcCRC	0011	Activates the CRC co-processor or performs a selftest.
Transmit	0100	Transmits data from the FIFO buffer.
NoCmd Change	0111	No command change. This command can be used to modify different bits in the command register without touching the command. E.g. Power-down.
Receive	1000	Activates the receiver circuitry.
Transceive	1100	Transmits data from FIFO buffer to the antenna and activates automatically the receiver after transmission.
-	1101	Reserved for further use
MFAuthent	1110	Performs the MIFARE® standard authentication as a reader
Soft Reset	1111	Resets the MFRC522

18.3.1 MFRC522 Command Description

18.3.1.1 Idle Command

The MFRC522 is in Idle mode. This command is also used to terminate the actual command.

18.3.1.2 Mem Command

Transfers 25 byte from the FIFO to the internal buffer.

To read out the 25 byte from the internal buffer, the command Mem with an empty FIFO buffer has to be started. In this case the 25 bytes are transferred from the internal buffer to the FIFO.

During a hard power down (reset pin) the 25 byte in the internal buffer remains unchanged but will be lost when supply power is removed from MFRC522.

This command terminates automatically when finished and the active command is idle.

18.3.1.3 Generate RandomID Command

This command generates a 10 byte random number stored in the internal buffer and overwrites the 10 bytes internal 25 byte buffer. This command terminates automatically when finished and the MFRC522 returns to idle.

18.3.1.4 CalcCRC Command

The content of the FIFO is transferred to the CRC co-processor and a CRC calculation is started. The result of this calculation is stored in the *CRCResultReg* register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped, when the FIFO gets empty during the data stream. The next byte written to the FIFO is added to the calculation.

The pre-set value of the CRC is controlled by the *CRCPreset* bits of the *ModeReg* register and the value is loaded to the CRC co-processor when the command is started.

This command has to be terminated by writing any command to register *CommandReg* e.g. the command Idle.

If the *SelfTest* bits in the register *AutoTestReg* are set correct, the MFRC522 is in Self Test mode and starting the CalCCRC command performs a digital selftest. The result of the selftest is written to the FIFO.

18.3.1.5 Transmit Command

The content of the FIFO is transmitted immediately after starting the command. Before transmitting the FIFO content all relevant register have to be set to transmit data.

This command terminates automatically when the FIFO gets empty. It can be terminated by any other command written to the command register.

18.3.1.6 NoCmdChange Command

This command does not influence any ongoing command in the *CommandReg* register. It can be used to manipulate any bit except the *command* bits in the *CommandReg* register, e.g. the bits *RcvOff* or *PowerDown*.

18.3.1.7 Receive Command

The MFRC522activates the receiver path and waits for any data stream to be received. The correct settings have to be chosen before starting this command.

This command terminates automatically when the received data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected framing and speed.

Remark: If the bit *RxMultiple* in the *RxModeReg* register is set to logic 1, the Receive command does not terminate automatically. It has to be terminated by activating any other command in the *CommandReg* register.

18.3.1.8 Transceive Command

This circular command repeats transmitting data from the FIFO and receiving data from the RF field continuously. The first action is transmitting and after a transmission the command is changed to receive a data stream.

Each transmission process has to be started by setting bit *StartSend* in the register *BitFramingReg* to logic 1. This command has to be cleared by software by writing any command to register *CommandReg* e.g. the command idle.

Remark: If the bit *RxMultiple* in register *RxModeReg* is set to logic 1, this command will never leave the receiving state, because the receiving will not be cancelled automatically.

18.3.1.9 MFAuthent Command

This command handles the MIFARE® authentication to enable a secure communication to any MIFARE® classic card. The following data shall be written to the FIFO before the command can be activated:

- Authentication command code (60h, 61h)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes shall be written to the FIFO.

Remark: When the MFAuthent command is active, any FIFO access is blocked. Anyhow if there is an access to the FIFO, the bit *WrErr* in the **ErrorReg** register is set.

This command terminates automatically when the MIFARE® card is authenticated and the bit *MFCrypto1On* in the *Status2Reg* register is set to logic 1.

This command does not terminate automatically when the card does not answer, therefore the timer should be initialized to automatic mode. In this case, beside the bit *IdleIrq*, the bit *TimerIrq* can be used as termination criteria. During authentication processing the bit *RxIrq* and bit *TxIrq* are blocked. The *Crypto1On* bit is only valid after termination of the authent command (either after processing the protocol or after writing IDLE to the command register).

In case there is an error during authentication, the bit *ProtocolErr* in the *ErrorReg* register is set to logic 1 and the bit *Crypto1On* in register *Status2Reg* is set to logic 0.

18.3.1.10 SoftReset Command

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command terminates automatically when finished.

Remark: The *SerialSpeedReg* register is reset and therefore the serial data rate is set to 9.6 kbps.

19. Testsignals

19.1 Selftest

The MFRC522 has the capability to perform a digital selftest. To start the selftest the following procedure has to be performed:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and perform the Config Command.
3. Enable the Selftest by writing the value 09h to the register *AutoTestReg*.
4. Write 00h to the FIFO.
5. Start the Selftest with the CalcCRC Command.
6. The Selftest will be performed.
7. When the Selftest is finished, the FIFO contains the following bytes:

Correct answer for register VersionReg equal to 90h:

```
00h, 87h, 98h, 0fh, 49h, FFh, 07h, 19h
BFh, 22h, 30h, 49h, 59h, 63h, ADh, CAh
7Fh, E3h, 4Eh, 03h, 5Ch, 4Eh, 49h, 50h
47h, 9Ah, 37h, 61h, E7h, E2h, C6h, 2Eh
75h, 5Ah, EDh, 04h, 3Dh, 02h, 4Bh, 78h
32h, FFh, 58h, 3Bh, 7Ch, E9h, 00h, 94h
B4h, 4Ah, 59h, 5Bh, FDh, U9h, 29h, DFh
35h, 96h, 98h, 9Eh, 4Fh, 30h, 32h, 8Dh
```

Correct answer for register VersionReg equal to 91h:

```
00h, C6h, 37h, D5h, 32h, B7h, 57h, 5Ch,
C2h, D8h, 7Ch, 4Dh, D9h, 70h, C7h, 73h,
10h, E6h, D2h, AAh, 5Eh, A1h, 3Eh, 5Ah,
14h, AFh, 30h, 61h, C9h, 70h, DBh, 2Eh,
64h, 22h, 72h, B5h, BDh, 65h, F4h, ECh,
22h, BCh, D3h, 72h, 35h, CDh, AAh, 41h,
1Fh, A7h, F3h, 53h, 14h, DEh, 7Eh, 02h,
D9h, 0Fh, B5h, 5Eh, 25h, 1Dh, 29h, 79h
```

19.2 Test bus

The test bus is implemented for production test purposes. The following configuration can be used to improve the design of a system using the MFRC522. The test bus allows to route internal signals to the digital interface. The test bus signals are selected by accessing *TestBusSel* in register *TestSel2Reg*.

Table 150: TestSel2Reg register (address 07h)

Pins	D6	D5	D4	D3	D2	D1
Testsignal	sdata	scoll	svalid	sover	RCV_reset	-

Table 151: Description of Testsignals

Pins	Testsignal	Description
D6	sdata	shows the actual received data stream.
D5	scoll	shows if in the actual bit a collision has been detected (106 kbit/s only)
D4	svalid	shows if sdata and scoll are valid
D3	sover	shows that the receiver has detected a stop condition
D2	RCV_reset	shows if the receiver is reset
D1	-	reserved

Table 152: TestSel2Reg register (address 0Dh)

Pins	D6	D5	D4	D3	D2	D1
Testsignal	clkstable	clk27/8	-	-	clk27	-

Table 153: Description of Testsignals

Pins	Testsignal	Description
D6	clkstable	shows if the oscillator delivers a stable signal.
D5	clk27/8	shows the output signal of the oscillator divided by 8
D4 to D3	-	reserved
D2	clk27	shows the output signal of the oscillator
D1	-	reserved

19.3 Testsignals at pin AUX

With the MFRC522, the user may select internal signals to measure them at pin AUX. These measurements can be helpful during the design-in phase to optimise the design or for test purpose.

Table 154 shows an overview of the signal that can be switched to pin AUX1 or AUX2 by setting *SelAux1* or *SelAux2* in the register *AnalogTestReg*.

Please also refer to register *AnalogSelAux*.

Remark: The DAC has a current output. It is recommended to use a 1 kΩ pull-down resistance at pins AUX1/AUX2.

Table 154: Testsignals description

SelAux	Description for Aux1 / Aux2
0000	Tristate
0001	DAC: register TestDAC 1/2
0010	DAC: testsignal corr1
0011	Reserved
0100	DAC: testsignal MinLevel
0101	DAC: ADC_I
0110	DAC: ADC_Q
0111 - 1001	Reserved
1010	High
1011	low

Table 154: Testsignals description

SelAux	Description for Aux1 / Aux2
1100	TxActive
1101	RxActive
1110	Subcarrier detected
1111	TstBusBit

19.3.1 Example: Output TestDAC 1 on AUX1 and TestDAC 2 on AUX2

Register *AnalogTestReg* is set to 11h. The output of AUX1 corresponds to the TestDAC 1 and the output of AUX2 to the TestDAC 2. The value of TestDAC 1 and TestDAC 2 is controlled by register *TestDAC1Reg* and *TestDAC2Reg*.

Figure 24 shows *TestDAC1Reg* programmed with a slope from 00h to 3Fh. *TestDAC2Reg* has been programmed with a rectangular signal with values of 00h and 3Fh.

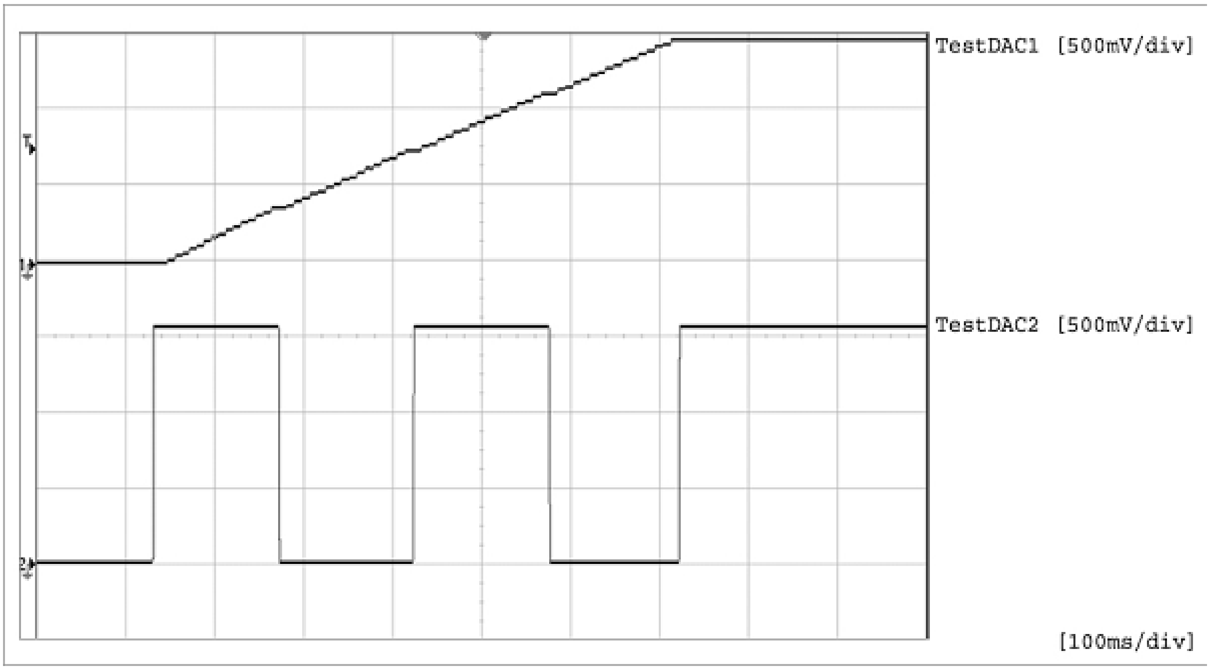


Fig 24. Output TestDAC 1 on AUX1 and TestDAC 2 on AUX2

19.3.2 Example: Output Testsignal Corr1 on AUX1 and MinLevel on AUX2

The following Figure 25 shows the test signal Corr 1 and the test signal MinLevel. The *AnalogTestReg* is set to 24h. The output of AUX1 corresponds to the Corr1 signal and AUX2 to the MinLevel.

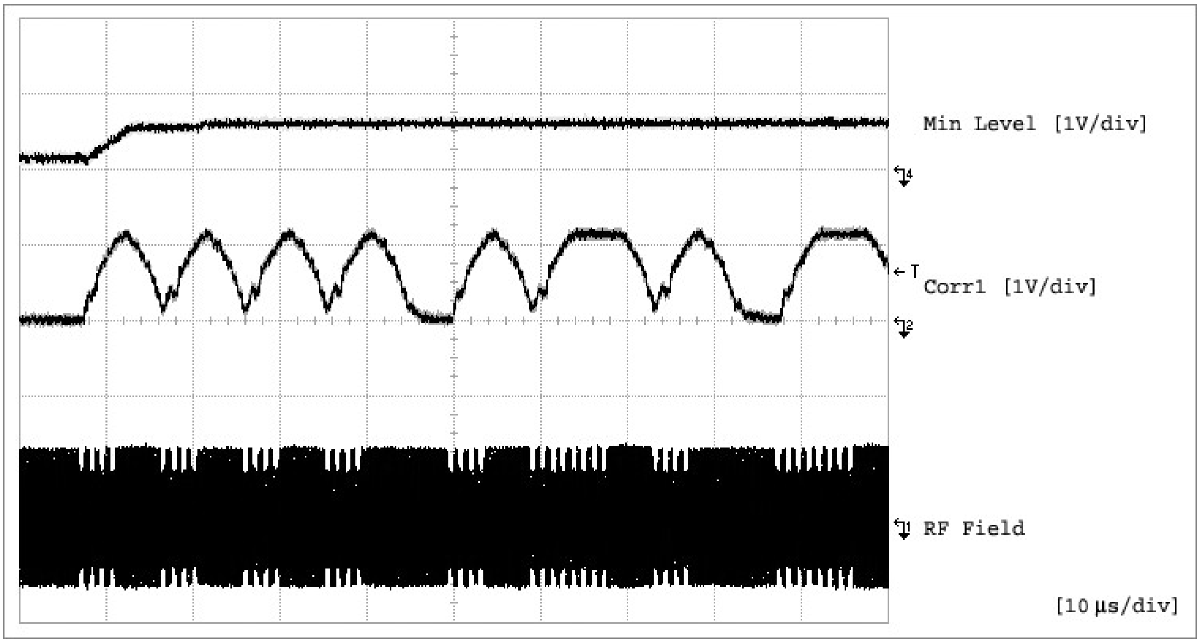


Fig 25. Output Testsignal Corr1 on AUX1 and MinLevel on AUX2.

19.3.3 Example: Output ADC channel I on AUX 1 and ADC channel Q on AUX 2

Figure 26 shows the ADC_I and ADC_Q channel behaviour. The *AnalogTestReg* is set to 56h.

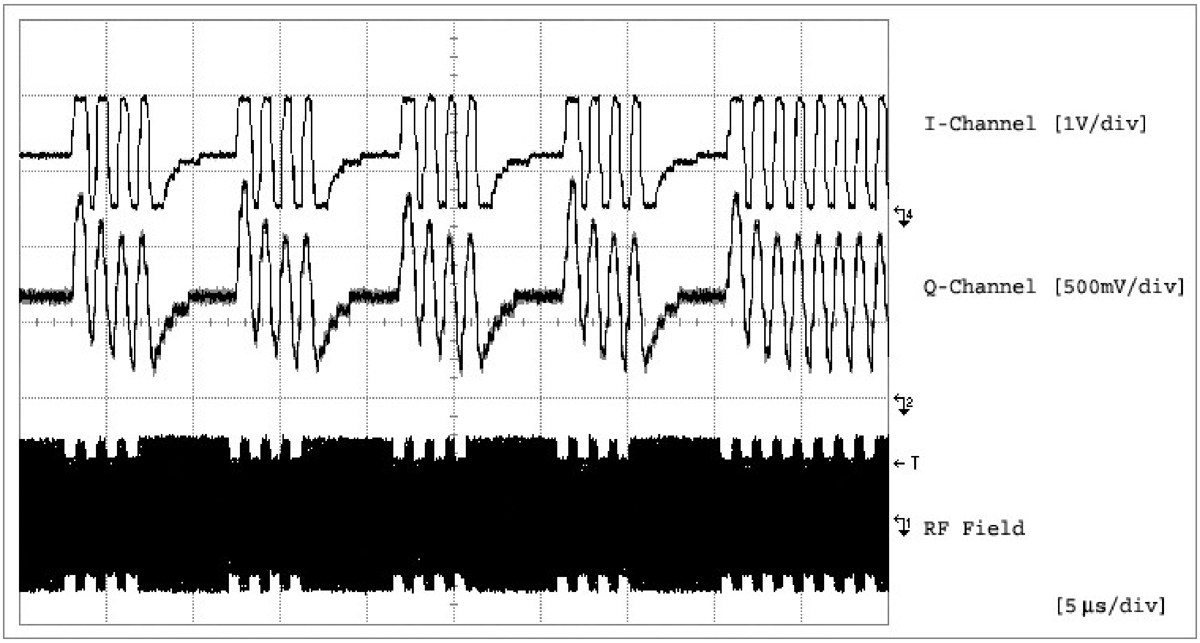


Fig 26. Output ADC channel I on AUX 1 and ADC channel Q on AUX 2.

19.3.4 Example: Output RxActive on AUX 1 and TxActive on AUX 2

The following Figure 27 shows the RXActive and TXActive signal in accordance to the RF communication. The *AnalogTestReg* was set to CDh.

Remark: At 106 kbit/s, RxActive is HIGH during databits, parity and CRC reception. Startbits are not included.
At 106 kbit/s, TxActive is HIGH during startbits, databits, parity and CRC transmission.
At 212, 424 and 848 kbit/s, RxActive is HIGH during datbits and CRC reseption. Startbits are not included.
At 212, 424 and 848 kbit/s, TxActive is HIGH during databits and CRC transmission.

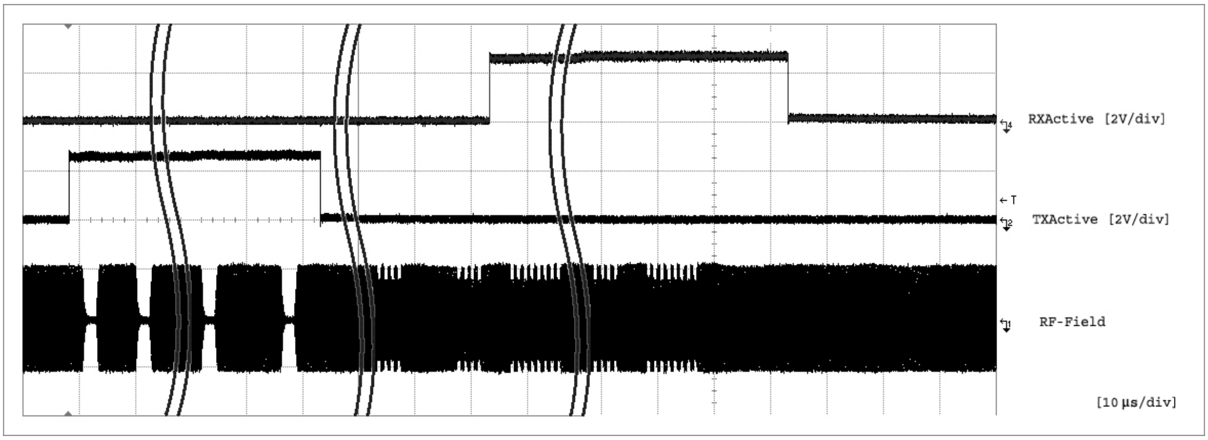


Fig 27. Output RxActive on AUX 1 and TxActive on AUX 2.

19.3.5 Example: Output Rx Data Stream on AUX 1 and AUX 2

The following Figure 28 shows the actual received data stream. *TestSel2Reg* is set to 07h to enable certain digital test data on D1-D6 (see Section 19.2 “Test bus”). The register *TestSel1Reg* is set to 06h (D6 = sdata) and *AnalogTestReg* is set to FFh to output the received data stream to pin AUX1 and AUX2.

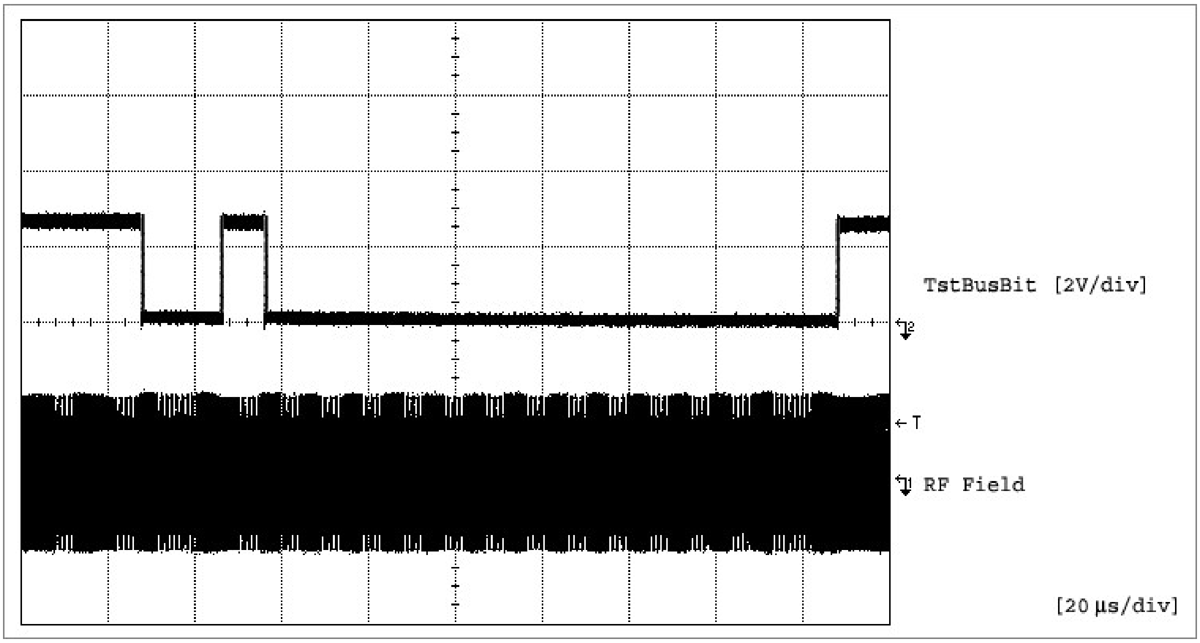


Fig 28. Output Rx data stream on AUX 1 and AUX 2.

19.4 PRBS (Pseudo-Random Binary Sequence)

Enables the PRBS9 or PRBS15 sequence according to ITU-TO150. To start the transmission of the defined datastream the command TRANSMIT has to be activated. The preamble/Sync byte/start bit/parity bit are generated automatically depending on the selected mode.

Remark: All relevant register to transmit data have to be configured before entering PRBS mode according ITU-TO150.

20. Limiting values

Table 155. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
AV_{DD} DV_{DD} PV_{DD} TV_{DD} SV_{DD}	Supply voltage		-0.5	+4.0	V
V_{in}	Input voltage	for all input-pins except MFIN and Rx	PV_{SS} -0.5	PV_{DD} +0.5	V
$V_{in,MFIN}$	Input voltage	for MFIN pin only	PV_{SS}-0.5	SV_{DD}+0.5	V
P_{tot}	Total power dissipation per package (V_{BUS} and DV_{DD} in short cut mode)		-	200	mW
T_J	Junction temperature range			100	°C
ESDH	ESD Susceptibility (Human Body model)	1500 Ω, 100 pF; JESD22-A114-B		2000	V
ESDM	ESD Susceptibility (Machine model)	0.75 µH, 200 pF; JESD22-A114-A		200	V

21. Recommended operating conditions

Table 156: Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	Ambient Temperature	HVQFN32		-25	-	+85	°C
AV_{DD} DV_{DD} TV_{DD}	Supply Voltage	$AV_{SS} = DV_{SS} = PV_{SS} = TV_S = 0$ V, $PV_{DD} \leq AV_{DD} = DV_{DD} = TV_{DD}$	[2]	2.5	3.3	3.6	V
PV_{DD}			[3]	1.6	1.8	3.6	V

[1] Supply voltages below 3 V reduces the performance (e.g. the achievable operating distance).

[2] AV_{DD}, DV_{DD} and TV_{DD} shall always be on the same voltage level.

[3] PV_{DD} shall always be on the same or lower voltage level than DV_{DD}.

22. Thermal characteristics

Table 157: Thermal characteristics

Symbol	Parameter	Conditions	Package	Typ	Unit
R_{thj-a}	Thermal resistance from junction to ambient	In still air with exposed pad soldered on a 4 layer Jedec PCB	HVQFN32	40	K/W

23. Characteristics

23.1 Input Pin Characteristics

23.1.1 Input Pin characteristics for pins EA, I2C and NRESET

Table 158: Input Pin characteristics for pins EA, I2C and NRESET

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 PV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 PV_{DD}	V

23.1.2 Input Pin characteristics for pin MFIN

Table 159: Input Pin characteristics for MFIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 SV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 SV_{DD}	V

23.1.3 Input/Output Pin characteristics for pins D1, D2, D3, D4, D5, D6 and D7

Table 160: Input/Output Pin characteristics for pins D1, D2, D3, D4, D5, D6 and D7

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 PV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 PV_{DD}	V
V_{OH}	Output voltage HIGH	PV_{DD} = 3 V, I_O = 4 mA	PV_{DD} -400 mV	-	PV_{DD}	V
V_{OL}	Output voltage LOW	PV_{DD} = 3 V, I_O = 4 mA	PV_{SS}	-	PV_{SS} +400 mV	V
I_{OH}	Output current drive HIGH	PV_{DD} = 3 V	-	-	4	mA
I_{OL}	Output current drive LOW	PV_{DD} = 3 V	-	-	4	mA

23.1.4 Input Pin characteristics for pin SDA

Table 161: Input Pin characteristics for pin SDA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA
V_{IH}	Input voltage High		0.7 PV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 PV_{DD}	V

23.1.5 Output Pin characteristics for Pin MFOUT

Table 162: Output Pin characteristics for Pin MFOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output voltage HIGH	SV_{DD} = 3 V, I_O = 4 mA	SV_{DD} -400 mV	-	SV_{DD}	V
V_{OL}	Output voltage LOW	SV_{DD} = 3 V, I_O = 4 mA	SV_{SS}	-	PV_{SS} +400 mV	V
I_{OL}	Output current drive LOW	SV_{DD} = 3 V	-	-	4	mA
I_{OH}	Output current drive HIGH	SV_{DD} = 3 V	-	-	4	mA

23.1.6 Output Pin characteristics for Pin IRQ

Table 163: Output Pin characteristics for Pin IRQ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output voltage HIGH	PV_{DD} = 3 V, I_O = 4 mA	PV_{DD} -400 mV	-	PV_{DD}	V
V_{OL}	Output voltage LOW	PV_{DD} = 3 V, I_O = 4 mA	PV_{SS}	-	PV_{SS} +400 mV	V
I_{OL}	Output current drive LOW	PV_{DD} = 3 V	-	-	4	mA
I_{OH}	Output current drive HIGH	PV_{DD} = 3 V	-	-	4	mA

23.1.7 Input Pin characteristics for Pin Rx

Table 164: Input Pin characteristics for Pin Rx

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN,RX}$	Input voltage range		-1	-	AV_{DD} +1 V	V
$C_{IN,RX}$	RX Input capacitance	AV_{DD} = 3 V, Receiver active, V_{RX} = 1 V_{PP}, 1.5 V_{DC} offset	-	10	-	pF
$R_{IN,RX}$	RX Input Series resistance	AV_{DD} = 3 V, Receiver active, V_{RX} = 1 V_{PP}, 1.5 V_{DC} offset	-	350	-	Ω

[1] The voltage on RX in clamped by internal diodes to AV_{SS} and AV_{DD}.

23.1.8 Input Pin characteristics for pin OSCIN

Table 165: Input Pin characteristics for OSCIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Leak}	Input Leakage current		-1	-	1	µA

Table 165: Input Pin characteristics for OSCIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage High		0.7 AV_{DD}	-	-	V
V_{IL}	Input voltage Low		-	-	0.3 AV_{DD}	V
C_{OSCIN}	Input capacitance	AV_{DD} = 2.8 V, V_{DC} = 0.65 V, V_{AC} = 1 V_{PP}	-	2	-	pF

23.1.9 Output Pin characteristics for Pins AUX1 and AUX2

Table 166: Output Pin characteristics for Pins AUX1 and AUX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output voltage HIGH	DV_{DD} = 3 V, I_O = 4 mA	DV_{DD} -400 mV	-	DV_{DD}	V
V_{OL}	Output voltage LOW	DV_{DD} = 3 V, I_O = 4 mA	DV_{SS}	-	DV_{SS} +400 mV	V
I_{OL}	Output current drive LOW	DV_{DD} = 3 V	-	-	4	mA
I_{OH}	Output current drive HIGH	DV_{DD} = 3 V	-	-	4	mA

23.1.10 Output Pin characteristics for Pins TX1 and TX2

Table 167: Output Pin characteristics for Pins TX1 and TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH,C32,3V}$	Output voltage HIGH	TV_{DD} = 3 V and I_{TX} = 32 mA, *CWGsP* = 3Fh	TV_{DD} -150 mV	-	-	mV
$V_{OH,C80,3V}$		TV_{DD} = 3 V and I_{TX} = 80 mA, *CWGsP* = 3Fh	TV_{DD} -400 mV	-	-	mV
$V_{OH,C32,2V5}$		TV_{DD} = 2.5 V and I_{TX} = 32 mA, *CWGsP* = 3Fh	TV_{DD} -240 mV	-	-	mV
$V_{OH,C80,2V5}$		TV_{DD} = 2.5 V and I_{TX} = 80 mA, *CWGsP* = 3Fh	TV_{DD} -640 mV	-	-	mV
$V_{OL,C32,3V}$	Output voltage LOW	TV_{DD} = 3 V and I_{TX} = 32 mA, *CWGsP* = 0Fh	-	-	150	mV
$V_{OL,C80,3V}$		TV_{DD} = 3 V and I_{TX} = 80 mA, *CWGsP* = 0Fh	-	-	400	mV
$V_{OL,C32,2V5}$		TV_{DD} = 2.5 V and I_{TX} = 32 mA, *CWGsP* = 0Fh	-	-	240	mV
$V_{OL,C80,2V5}$		TV_{DD} = 2.5 V and I_{TX} = 80 mA, *CWGsP* = 0Fh	-	-	640	mV

23.2 Current Consumption

Table 168: Current Consumption

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{HPD}	Hard Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, N_{RESET} = LOW	[4]	-	-	5	µA
I_{SPD}	Soft Power-down Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V	[4]	-	-	10	µA
I_{DVDD}	Digital Supply Current	$DV_{DD} = 3$ V		-	6.5	9	mA
I_{AVDD}	Analog Supply Current	$AV_{DD} = 3$ V, bit *RCVOff* = 0		-	7	10	mA
$I_{AVDD,RCVOFF}$	Analog Supply Current, receiver switched off	$AV_{DD} = 3$ V, bit *RCVOff* = 1		-	3	5	mA
I_{PVDD}	Pad Supply Current		[2]	-	-	40	mA
I_{TVDD}	Transmitter Supply Current	Continuous Wave	[1][3]	-	60[5]	100	mA
I_{SVDD}	MFIN/MFOUT Pad Supply Current		[6]	-	-	4	mA

[1] I_{TVDD} depends on TV_{DD} and the external circuitry connected to Tx1 and Tx2

[2] I_{PVDD} depends on the overall load at the digital pins.

[3] During operation with a typical circuitry the overall current is below 100 mA.

[4] I_{SPD} and I_{HPD} are the total currents over all supplies.

[5] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between TX1 and TX2 at 13.56 MHz

[6] I_{SVDD} depends on the load at the MFOUT pin.

23.3 RX Input Voltage Range

Table 169: RX Input Voltage Range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RX,MinIV,Man}$	Minimum Input voltage, Manchester Coded	AV_{DD} = 3 V	-	100	-	mVpp
$V_{RX,MaxIV,Man}$	Maximum Input voltage, Manchester Coded	AV_{DD} = 3 V	-	4	-	Vpp

Figure 29 outlines the voltage definitions.

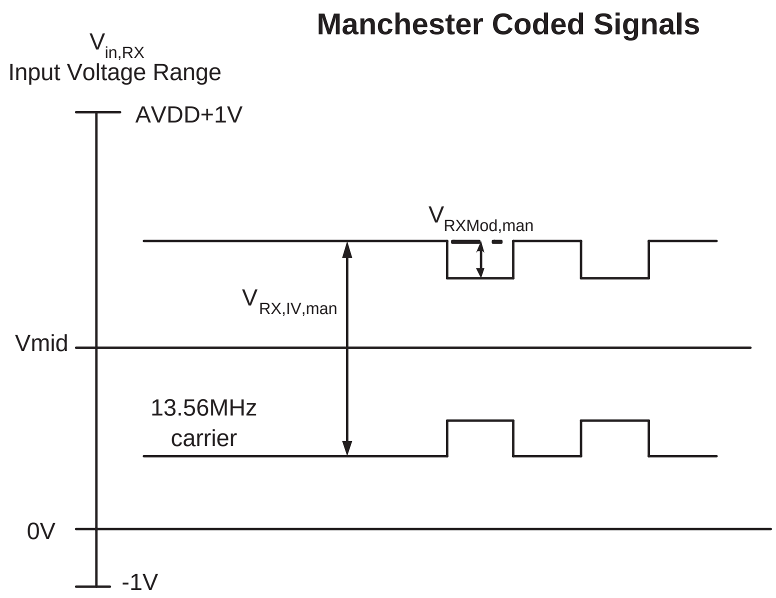


Fig 29. RX Input Voltage Range

23.4 RX Input Sensitivity

Table 170: RX Input Sensitivity

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RXMod,Man}$	Minimum modulation voltage	AV_{DD} = 3 V, RxGain = 7	-	5	-	mV

Figure 29 outlines the voltage definitions.

23.5 Clock Frequency

Table 171: Clock Frequency

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSCIN}	Clock Frequency		-	27.12	-	MHz
d_{FEC}	Duty Cycle of Clock Frequency		40	50	60	%
t_{jitter}	Jitter of Clock Edges		-	-	10	ps, RMS

23.6 XTAL Oscillator

Table 172: XTAL Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH,OSCOUT}$	Output Voltage High XTAL2		-	1.1	-	V
$V_{OL,OSCOUT}$	Output Voltage Low XTAL2		-	0.2	-	V
$C_{IN,OSCOUT}$	Input capacitance OSCOUT		-	2	-	pF
$C_{IN,OSCIN}$	Input capacitance OSCIN		-	2	-	pF

23.7 Typical 27.12 MHz Crystal Requirements

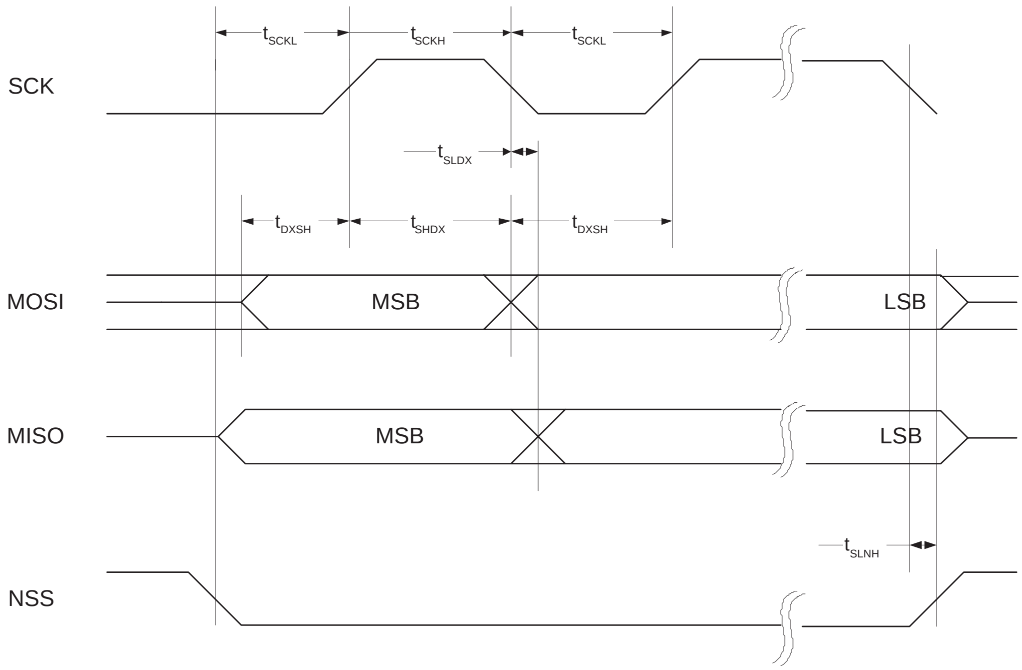
Table 173: XTAL Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTAL}	XTAL Frequency Range		-	27.12	-	MHz
ESR	XTAL Equivalent Series resistance		-	-	100	Ω
C_L	XTAL Load capacitance		-	10	-	pF
P_{XTAL}	XTAL Drive Level		-	50	100	W

23.8 Timing for the SPI compatible interface

Table 174: Timing Specification for SPI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SCKL}	SCK low pulse width		50		-	ns
t_{SCKH}	SCK high pulse width		50		-	ns
t_{SHDX}	SCK high to data changes		25		-	ns
t_{DXSH}	data changes to SCK high		25		-	ns
t_{SLDX}	SCK low to data changes		-		25	ns
t_{SLNH}	SCK low to NSS high		0		-	ns



Remark: The signal NSS has to be low to be able to send several bytes in one datastream.

To send more than one datastream NSS has to be set to HIGH level in between the data streams.

Fig 30. Timing Diagram for SPI.

23.9 I^{2}C Timing

Table 175. Overview I^{2}C Timing in Fast mode

Symbol	Parameter	Fast mode		High speed mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	400	0	3400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	600	-	160	-	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	600	-	160	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	600	-	160	-	ns
t_{LOW}	LOW period of the SCL clock	1300	-	160	-	ns
t_{HIGH}	HIGH period of the SCL clock	600	-	60	-	ns
$t_{HD;DAT}$	Data hold time	0	900	0	70	ns
$t_{SU;DAT}$	Data set-up time	100	-	10	-	ns
t_{rscl}	Rise time SCL signals	20	300	10	40	ns
t_{fscl}	Fall time SCL signals	20	300	10	40	ns
t_{rsda}	Rise time of both SDA and SCL signals	20	300	10	80	ns
t_{fsda}	Fall time of both SDA and SCL signals	20	300	10	80	ns
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	1.3	-	µs

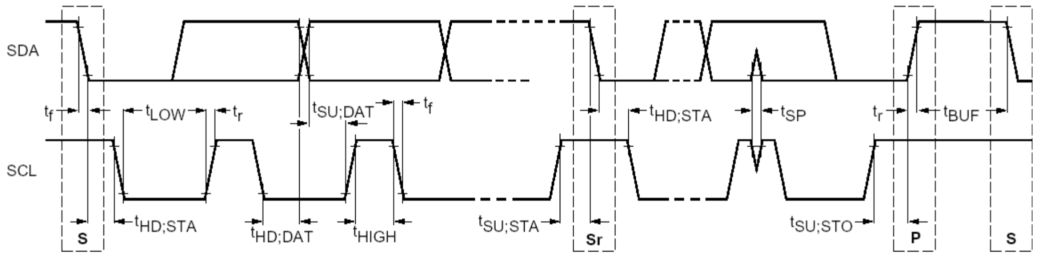


Fig 31. Timing for F/S mode devices on the I^{2}C-bus.

24. Application information

The figure below shows a typical circuit diagram, using a complementary antenna connection to the MFRC522.

The antenna tuning and RF part matching is described in the application note Ref. 1 and Ref. 2.

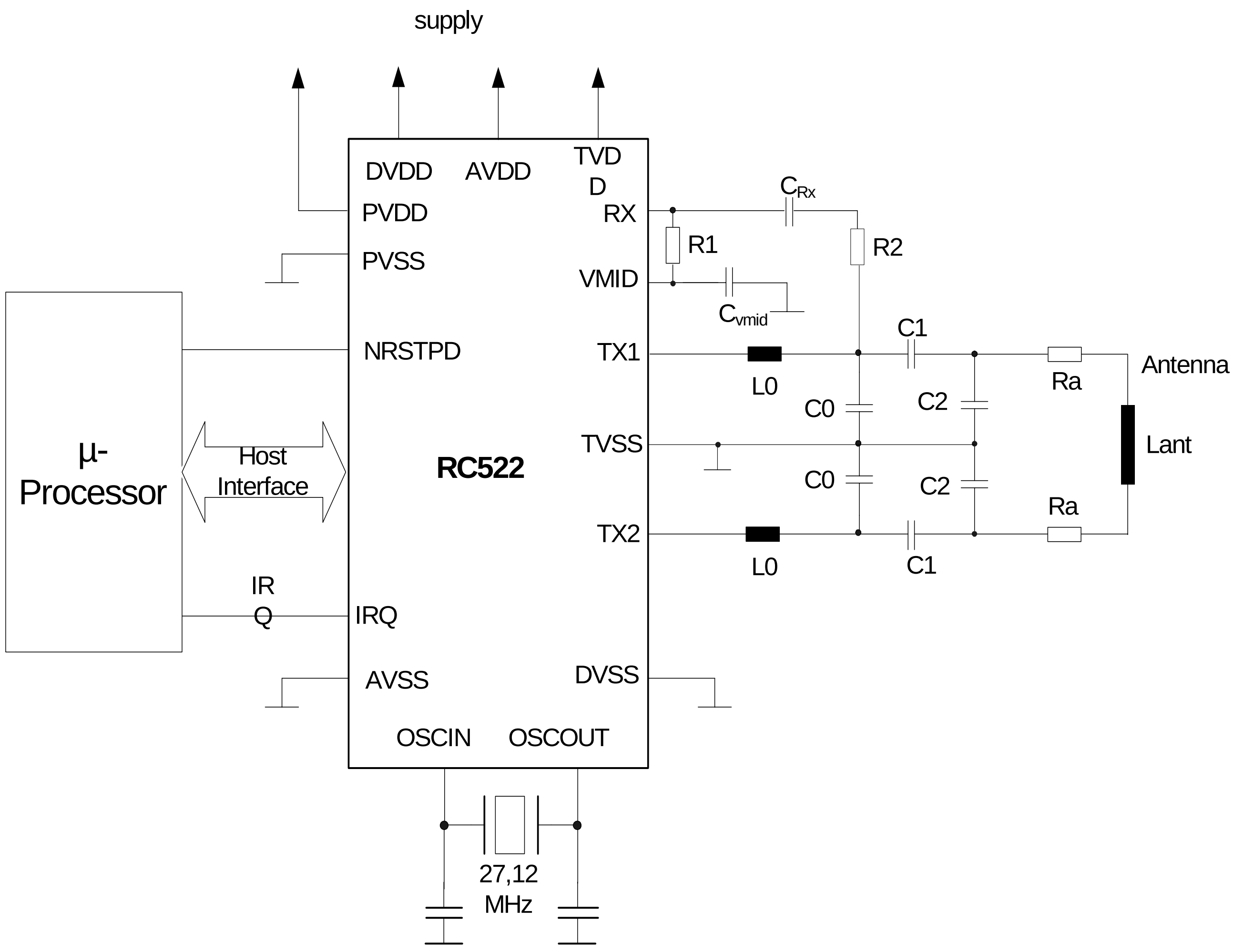
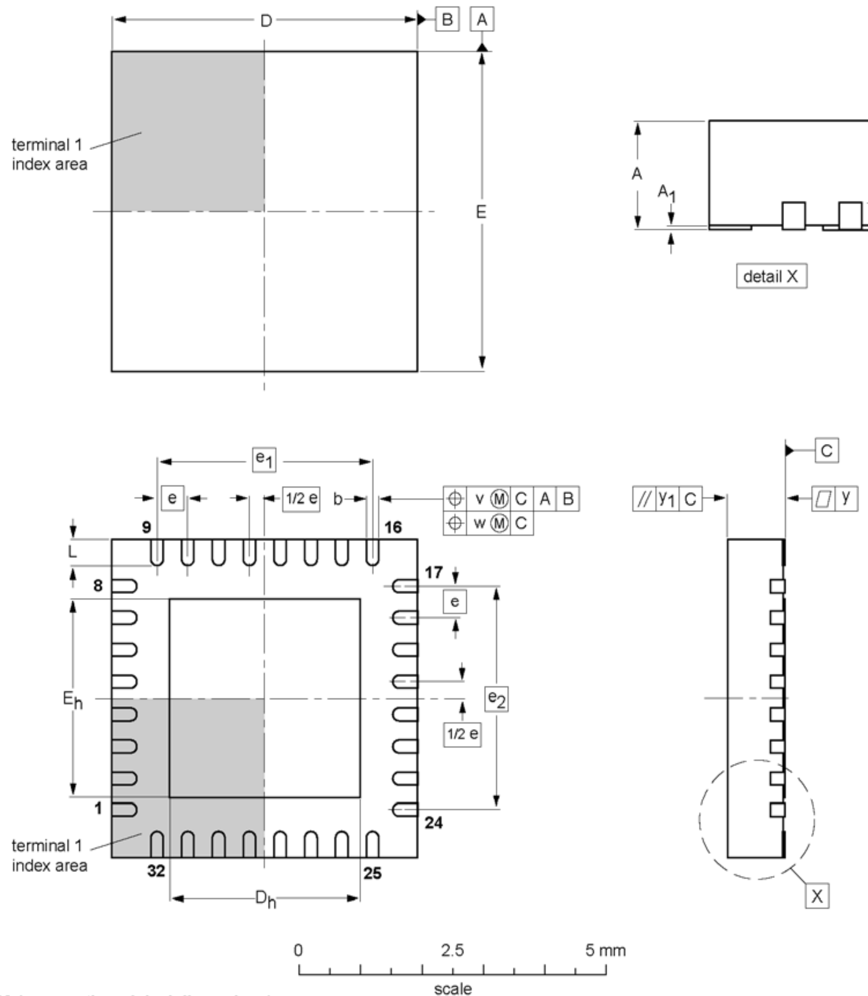


Fig 32. Typical Application Circuit Diagram

25. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 33. Package outline package version (HVQFN32)

Detailed package information can be found on NXP Internet
http://www.nxp.com/package/SOT617-1.html

26. Handling information

Moisture Sensitivity Level (MSL) Evaluation has been performed according to SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C). MSL for this package is level 1 which means 260 °C convection reflow temperature.

Dry pack is not required.

Unlimited out of pack Floor Life at maximum ambient 30 °C/85%RH.

27. Packing information

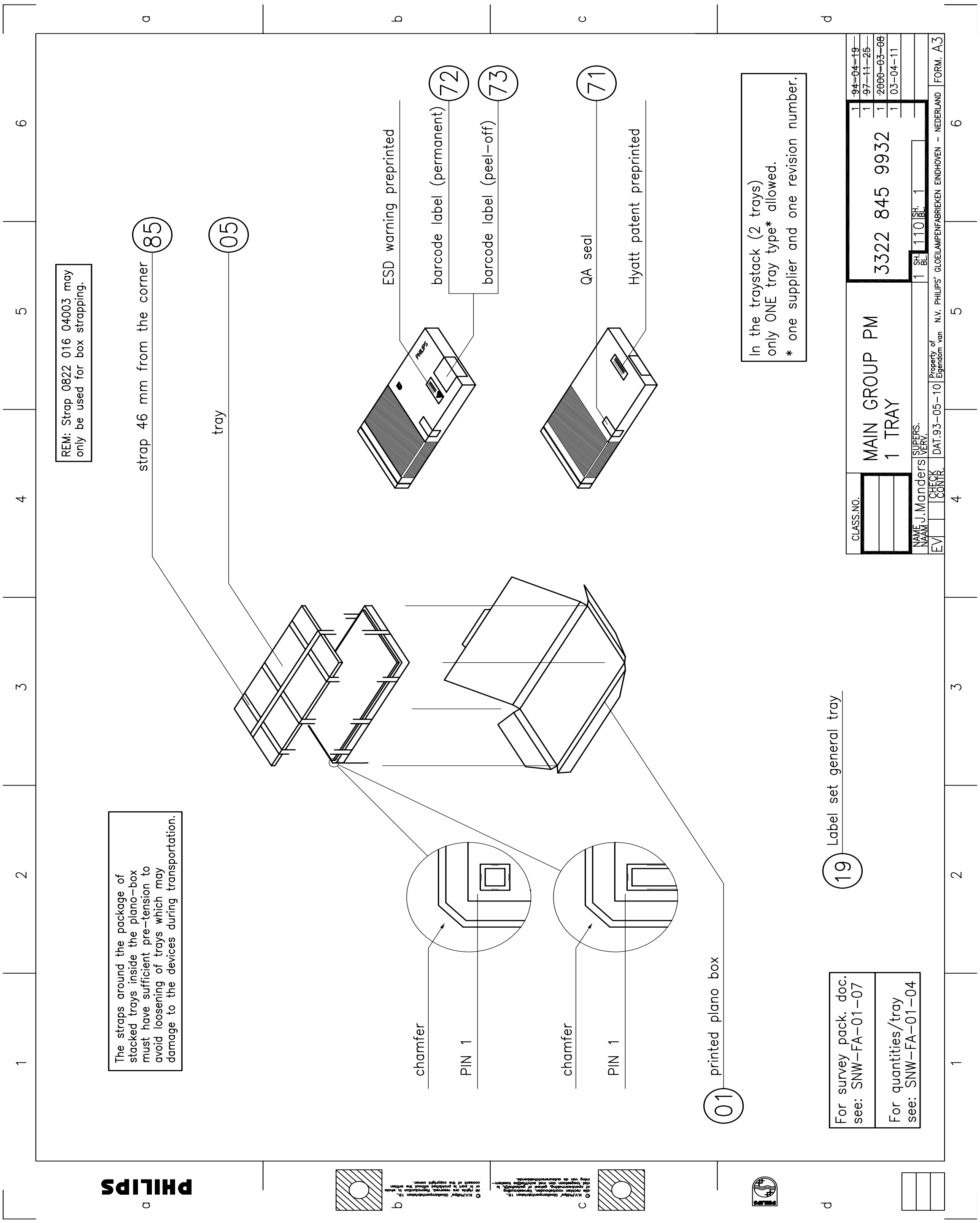


Fig 34. Packing Information 1 Tray

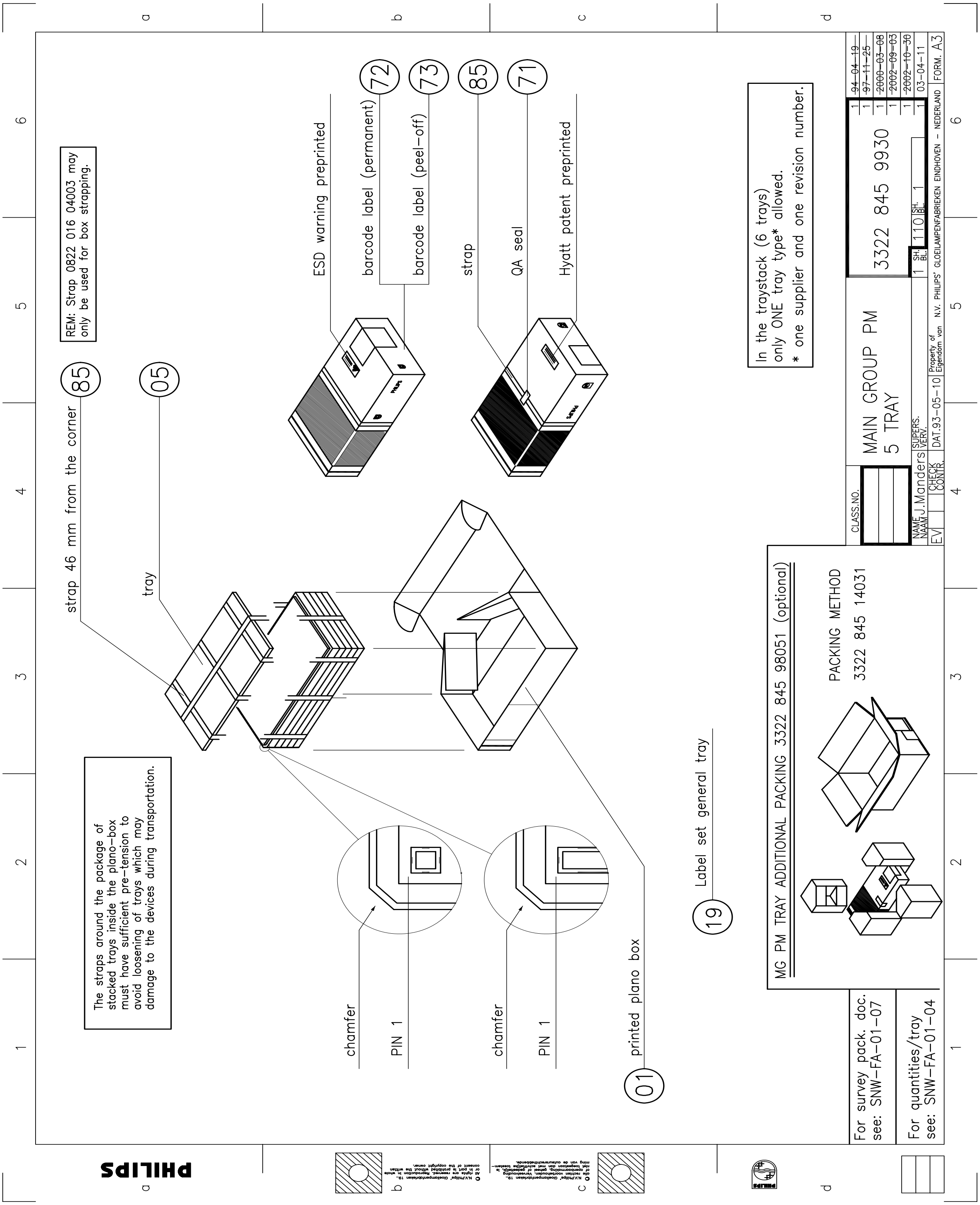


Fig 35. Packing Information 5Tray

28. Abbreviations

Table 176: Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
PCD	Proximity Coupling Device. Definition for a Card reader/writer according to the ISO/IEC 14443 specification.
PICC	Proximity Cards. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification.
PCD Æ PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443A/MIFARE®
PICCÆ PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443A/MIFARE®.
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin).
Loadmodulation Index	The load modulation index is defined as the card’s voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) measured at the card’s coil.

29. References

[1] **AN - MFRC52x Reader IC Family Directly Matched Antenna Design —** Application note for Mifare MFRC52x Reader IC Antenna Design

[2] **AN - Mifare(14443A) 13,56 MHz RFID Proximity Antennas —** Application note for Mifare Proximity Antenna Design

30. Revision history

Table 177: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
112132	Mai 2007	Product datasheet	200705005F		Revision 3.1
	• correction Interface PIN order in Table 135 “Connection Scheme for detecting the different Interface Types” • correction Table 137 • removed D0 from Table 150, Table 151, Table 152, Table 153 • removed 212, 424, 848 kbaud from Table 169 • correction typical application circuit diagram Figure 32 • add selftest answer for version reg. 91h in Section 19.1 “Selftest” (see CPCN 200705005F)				
112131	September 2006	Product datasheet			Revision 3.0
	• Introduction new NXP data sheet layout • Add Section 4 “Quick reference data” • Characterization up to 848 kbit/s • Add notes to Table 3 “Pin description” • Correction RFU description in Table 6 “Behavior of Register Bits and its Designation” • Correction access rights of bits 6-4 and 2-0 in Table 33 “BitFramingReg register (address 0Dh); reset value: 00h” • Correction DTRQ to Output in Table 135 “Connection Scheme for detecting the different Interface Types” • Combined “Absolute Maximum Ratings” and “ESD Characteristics“ in Section 20 “Limiting values” • Renamed Table 161 “Input Pin characteristics for pin SDA” and delete “V_{OL} and I_{OL}“				
112130	December 2005	Product data sheet			Revision 2.1
	• Document status changed to product specification • Change Ordering Information Chapter 5 • Add Handling Information Chapter 26 • Add Packing Information Chapter 27 • Add Test Signal Examples in Chapter 19.3				
112121	September 2005				Revision 2.0
	• TxSelReg - bit DriverSel - combination 10				
112120	July 2005	Preliminary data sheet			Revision 1.0
	• Document status chacnged to preliminary specification • add package web-link (chapter 25) • add ordering information (chapter 5)				
112110	July 2005	Objective data sheet			Revision 0.4
	• Document status changed to objective specification • changes in various register descriptions • SVDD Pin (chapter 7.2) • ParityDisable bit (chapter 9.2.1.14) • add MFIN / MFOUT description (chapter 11.4) • various spelling corrections				
112104	November 2004				Revision 0.3

Table 177: Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
	• temporary remove type ordering information • changes in register description • adaptation figure 22				
112103	October 2004				
	• changes in register description				

31. Legal information

31.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Notes

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33. Tables

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34. Figures

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Document identifier: 112132

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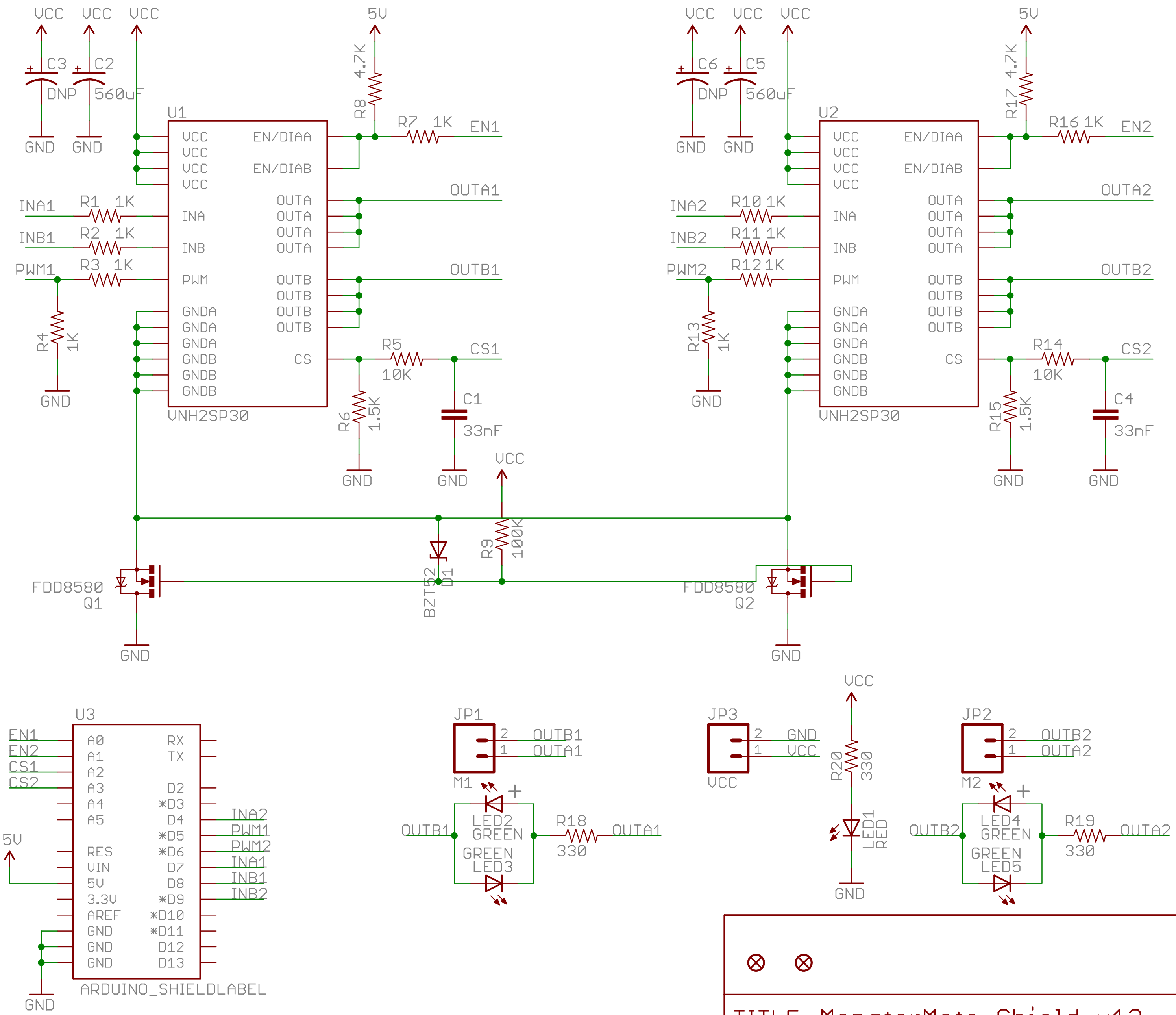

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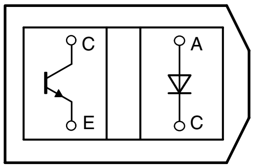
Document Number:	REV:
Date: 11/3/2010 12:02:08 PM	Sheet: 1/1

Reflective Optical Sensor with Transistor Output

19156_2



Top view

19156_1

DESCRIPTION

The TCRT5000 and TCRT5000L are reflective sensors which include an infrared emitter and phototransistor in a leaded package which blocks visible light. The package includes two mounting clips. TCRT5000L is the long lead version.

FEATURES

- Package type: leaded
- Detector type: phototransistor
- Dimensions (L x W x H in mm): 10.2 x 5.8 x 7
- Peak operating distance: 2.5 mm
- Operating range within > 20 % relative collector current: 0.2 mm to 15 mm
- Typical output current under test: $I_C = 1$ mA
- Daylight blocking filter
- Emitter wavelength: 950 nm
- Lead (Pb)-free soldering released
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

Pb-free
e2
RoHS
COMPLIANT

APPLICATIONS

- Position sensor for shaft encoder
- Detection of reflective material such as paper, IBM cards, magnetic tapes etc.
- Limit switch for mechanical motions in VCR
- General purpose - wherever the space is limited

PRODUCT SUMMARY

PART NUMBER	DISTANCE FOR MAXIMUM CTR_{rel} (1) (mm)	DISTANCE RANGE FOR RELATIVE $I_{out} > 20$ % (mm)	TYPICAL OUTPUT CURRENT UNDER TEST (2) (mA)	DAYLIGHT BLOCKING FILTER INTEGRATED
TCRT5000	2.5	0.2 to 15	1	Yes
TCRT5000L	2.5	0.2 to 15	1	Yes

Notes

(1) CTR: current transfere ratio, I_{out}/I_{in}

(2) Conditions like in table basic charactristics/sensors

ORDERING INFORMATION

ORDERING CODE	PACKAGING	VOLUME (1)	REMARKS
TCRT5000	Tube	MOQ: 4500 pcs, 50 pcs/tube	3.5 mm lead length
TCRT5000L	Tube	MOQ: 2400 pcs, 48 pcs/tube	15 mm lead length

Note

(1) MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (1)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
INPUT (EMITTER)				
Reverse voltage		V_R	5	V
Forward current		I_F	60	mA
Forward surge current	$t_p \leq 10$ µs	I_{FSM}	3	A
Power dissipation	$T_{amb} \leq 25$ °C	P_V	100	mW
Junction temperature		T_j	100	°C

ABSOLUTE MAXIMUM RATINGS [1]				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
OUTPUT (DETECTOR)				
Collector emitter voltage		V_{CEO}	70	V
Emitter collector voltage		V_{ECO}	5	V
Collector current		I_C	100	mA
Power dissipation	$T_{amb} \leq 55$ °C	P_V	100	mW
Junction temperature		T_j	100	°C
SENSOR				
Total power dissipation	$T_{amb} \leq 25$ °C	P_{tot}	200	mW
Ambient temperature range		T_{amb}	- 25 to + 85	°C
Storage temperature range		T_{stg}	- 25 to + 100	°C
Soldering temperature	2 mm from case, t ≤ 10 s	T_{sd}	260	°C

Note

(1) T_{amb} = 25 °C, unless otherwise specified

ABSOLUTE MAXIMUM RATINGS

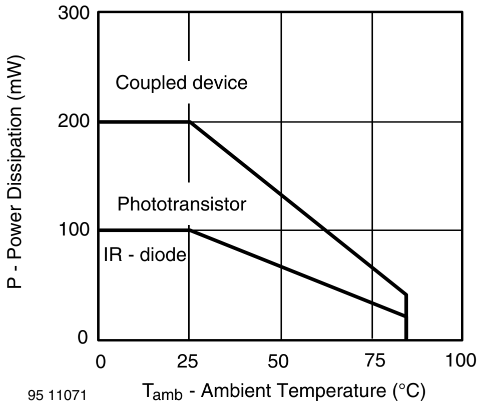


Fig. 1 - Power Dissipation Limit vs. Ambient Temperature

BASIC CHARACTERISTICS [1]						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
INPUT (EMITTER)						
Forward voltage	I_F = 60 mA	V_F		1.25	1.5	V
Junction capacitance	V_R = 0 V, f = 1 MHz	C_j		17		pF
Radiant intensity	I_F = 60 mA, t_p = 20 ms	I_e			21	mW/sr
Peak wavelength	I_F = 100 mA	λ_P	940			nm
Virtual source diameter	Method: 63 % encircled energy	d		2.1		mm
OUTPUT (DETECTOR)						
Collector emitter voltage	I_C = 1 mA	V_{CEO}	70			V
Emitter collector voltage	I_e = 100 µA	V_{ECO}	7			V
Collector dark current	V_{CE} = 20 V, I_F = 0 A, E = 0 lx	I_{CEO}		10	200	nA
SENSOR						
Collector current	V_{CE} = 5 V, I_F = 10 mA, D = 12 mm	I_C (2) (3)	0.5	1	2.1	mA
Collector emitter saturation voltage	I_F = 10 mA, I_C = 0.1 mA, D = 12 mm	V_{CEsat} (2) (3)			0.4	V

Note

(1) T_{amb} = 25 °C, unless otherwise specified

(2) See figure 3

(3) Test surface: mirror (Mfr. Spindler a. Hoyer, Part No. 340005)

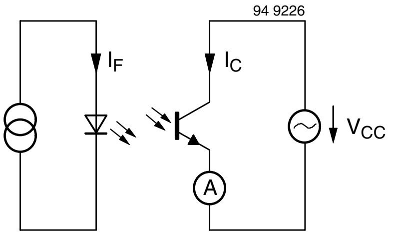


Fig. 2 - Test Circuit

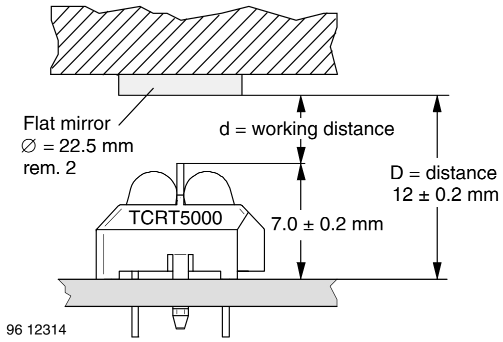


Fig. 3 - Test Circuit

BASIC CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified

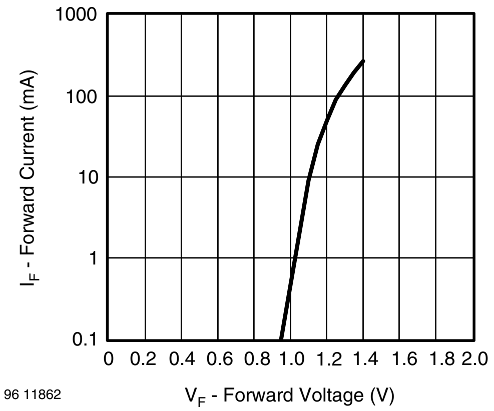


Fig. 4 - Forward Current vs. Forward Voltage

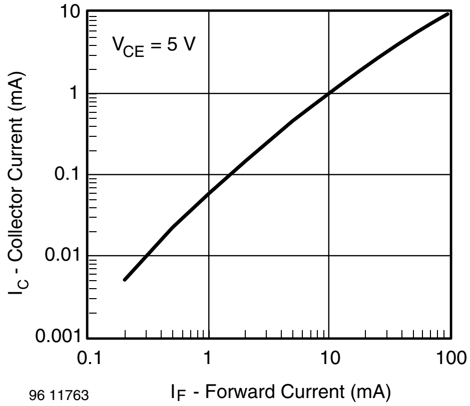


Fig. 6 - Collector Current vs. Forward Current

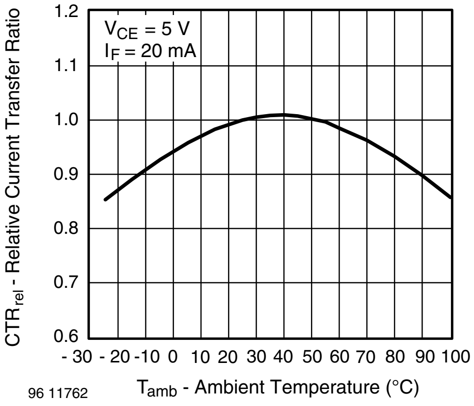


Fig. 5 - Relative Current Transfer Ratio vs. Ambient Temperature

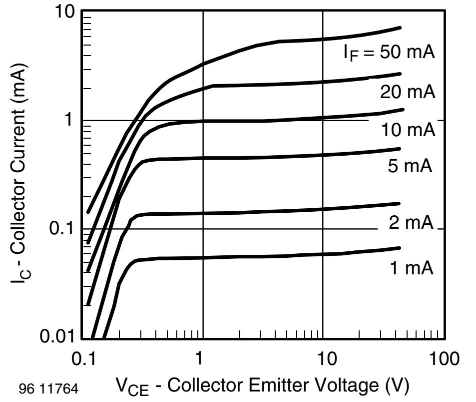


Fig. 7 - Collector Emitter Saturation Voltage vs. Collector Current

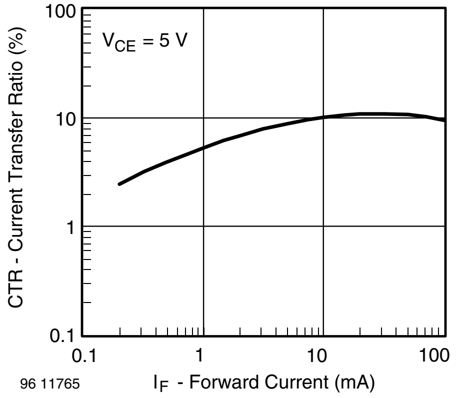


Fig. 8 - Current Transfer Ratio vs. Forward Current

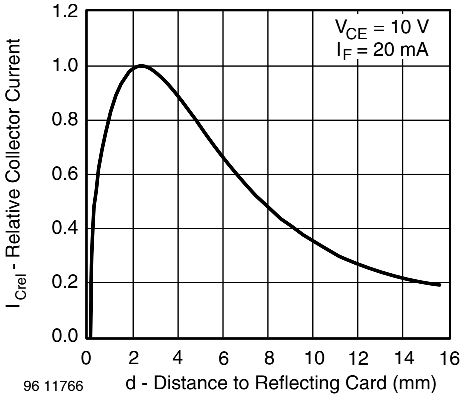
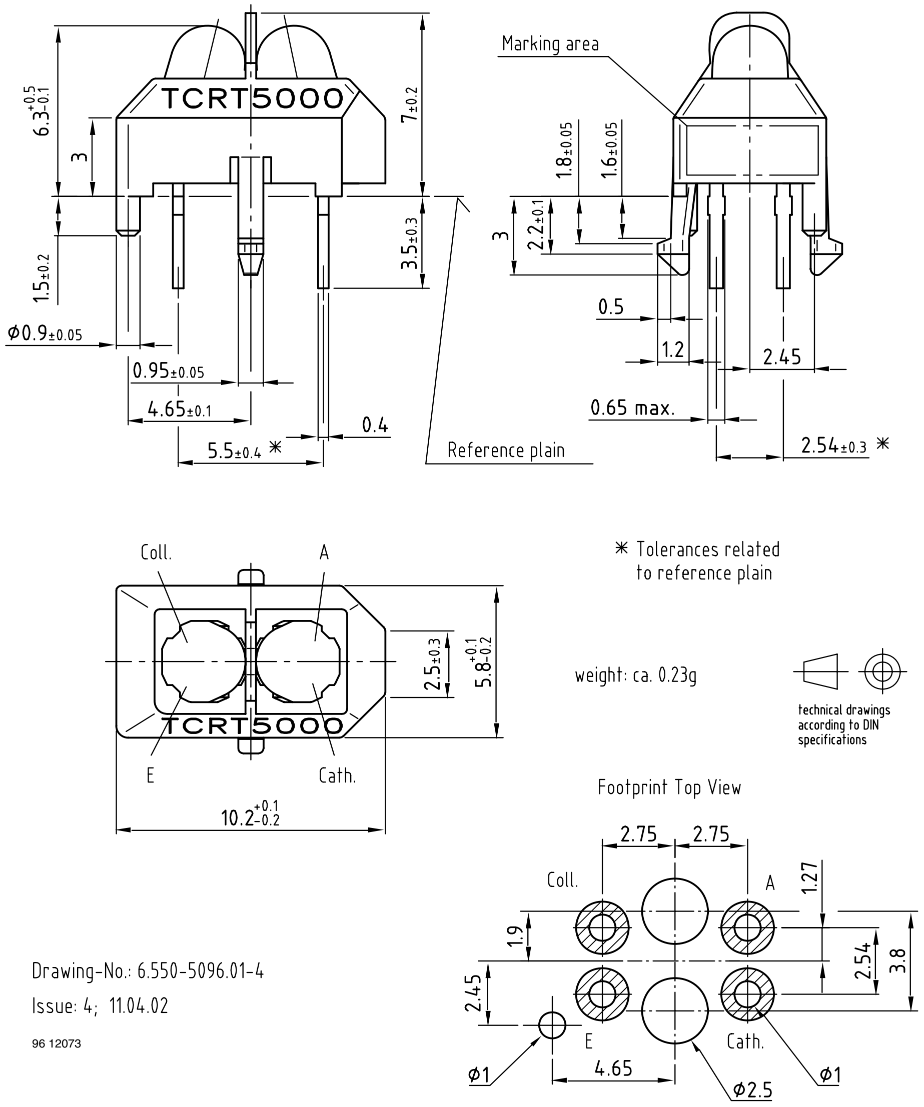
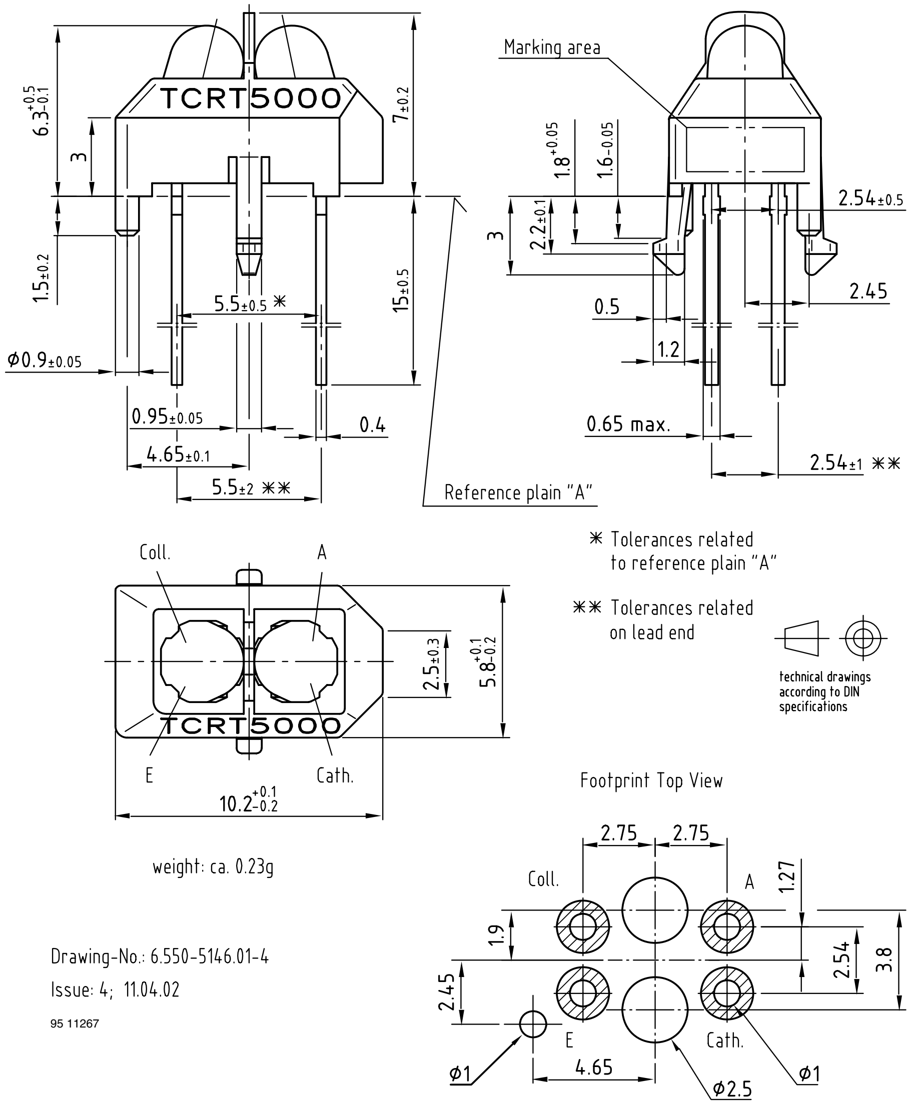


Fig. 9 - Relative Collector Current vs. Distance

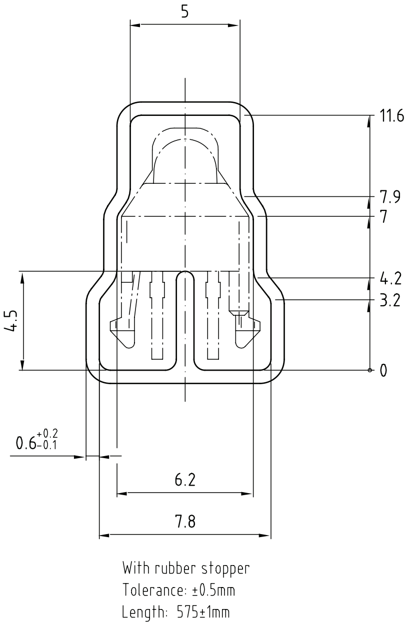
PACKAGE DIMENSIONS in millimeters, **TCRT5000**



PACKAGE DIMENSIONS in millimeters, **TCRT5000L**

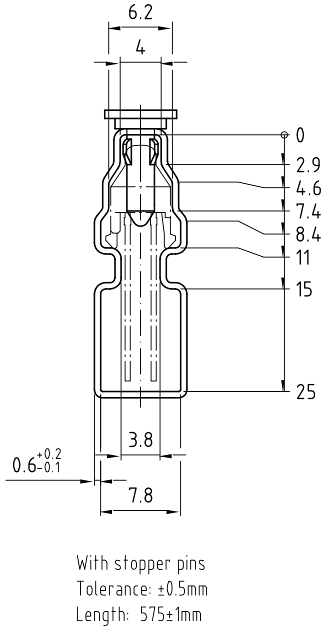


TUBE DIMENSIONS in millimeters, **TCRT5000**



Drawing-No.: 9.700-5139.01-4
Issue: 1; 10.05.00
20298

TUBE DIMENSIONS in millimeters, **TCRT5000L**



Drawing-No.: 9.700-5178.01-4
Issue: 1; 25.02.00
20299

Packaging and Ordering Information

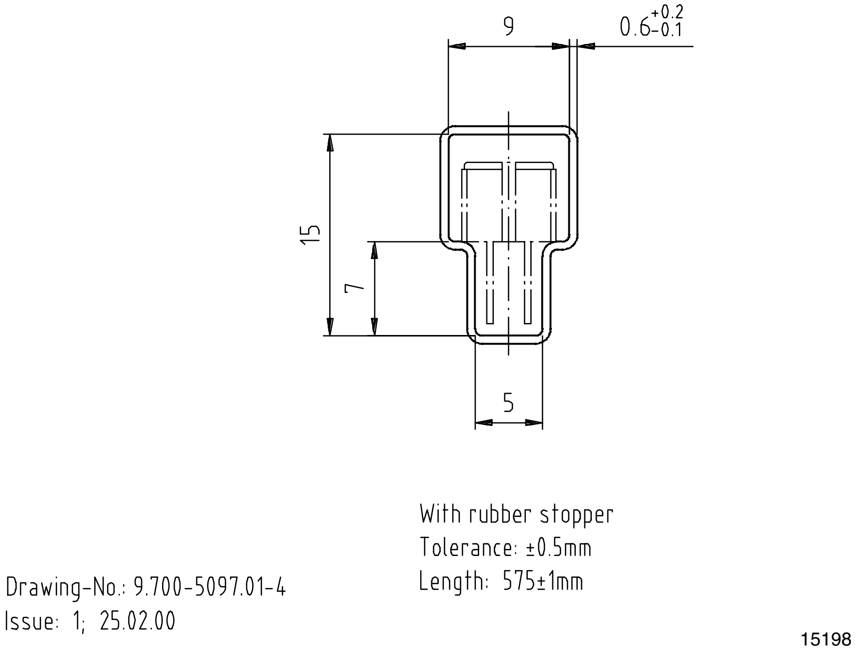
PART NUMBER	MOQ [1]	PCS PER TUBE	TUBE SPEC. (FIGURE)	CONSTITUENTS (FORMS)
CNY70	4000	80	1	28
TCPT1300X01	2000	Reel	[2]	29
TCRT1000	1000	Bulk	-	26
TCRT1010	1000	Bulk	-	26
TCRT5000	4500	50	2	27
TCRT5000L	2400	48	3	27
TCST1030	5200	65	5	24
TCST1030L	2600	65	6	24
TCST1103	1020	85	4	24
TCST1202	1020	85	4	24
TCST1230	4800	60	7	24
TCST1300	1020	85	4	24
TCST2103	1020	85	4	24
TCST2202	1020	85	4	24
TCST2300	1020	85	4	24
TCST5250	4860	30	8	24
TCUT1300X01	2000	Reel	[2]	29
TCZT8020-PAER	2500	Bulk	-	22

Notes

[1] MOQ: minimum order quantity

[2] Please refer to datasheets

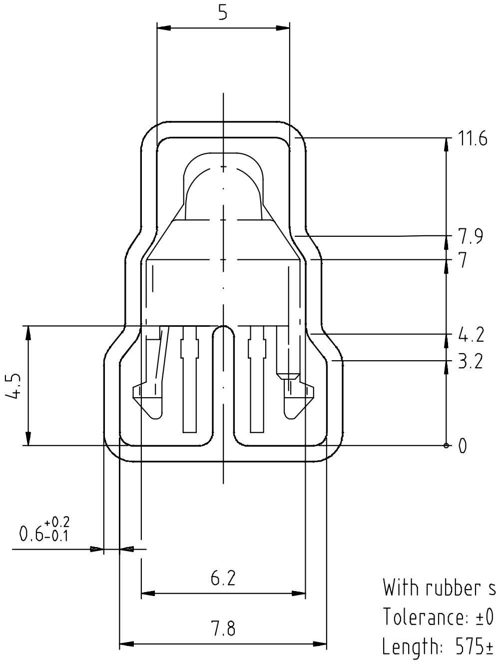
TUBE SPECIFICATION FIGURES



With rubber stopper
Tolerance: ±0.5mm
Length: 575±1mm

Drawing-No.: 9.700-5097.01-4
Issue: 1; 25.02.00

Fig. 1



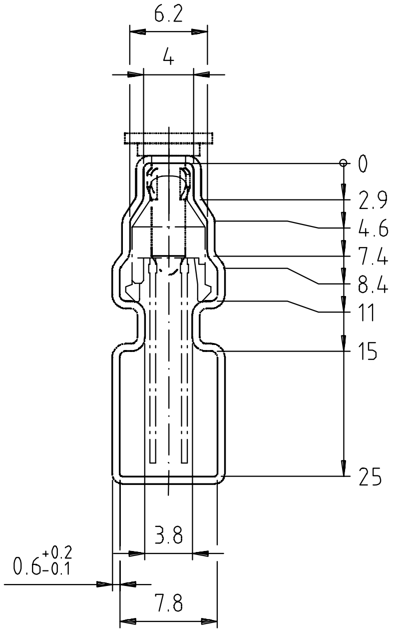
With rubber stopper
Tolerance: ±0.5mm
Length: 575±1mm

Drawing-No.: 9.700-5139.01-4
Issue: 1; 10.05.00

Drawing refers to following types: TCRT 5000

15210

Fig. 2

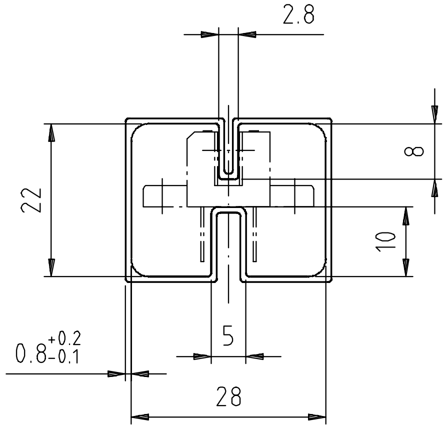


With stopper pins
Tolerance: ±0.5mm
Length: 575±1mm

Drawing-No.: 9.700-5178.01-4
Issue: 1; 25.02.00

15201

Fig. 3

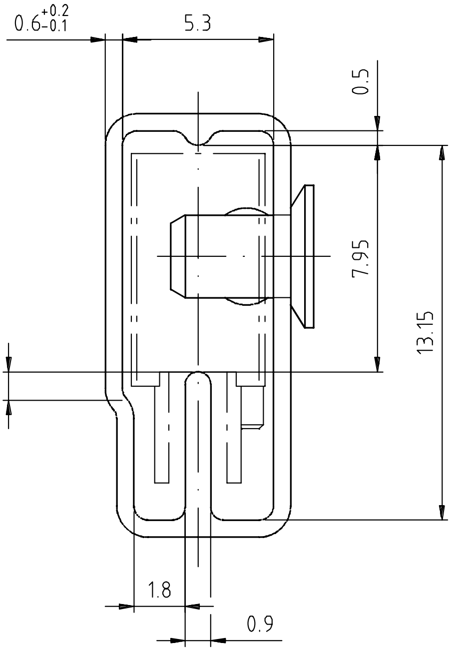


With rubber stopper
Tolerance: ±0.5mm
Length: 575±1mm

Drawing-No.: 9.700-5100.01-4
Issue: 1; 25.02.00

15199

Fig. 4



With stopper pins
Tolerance: ±0.5mm
Length: 575±1mm

Drawing-No.: 9.700-5140.01-4
Issue: 1; 25.02.00

15202

Fig. 5

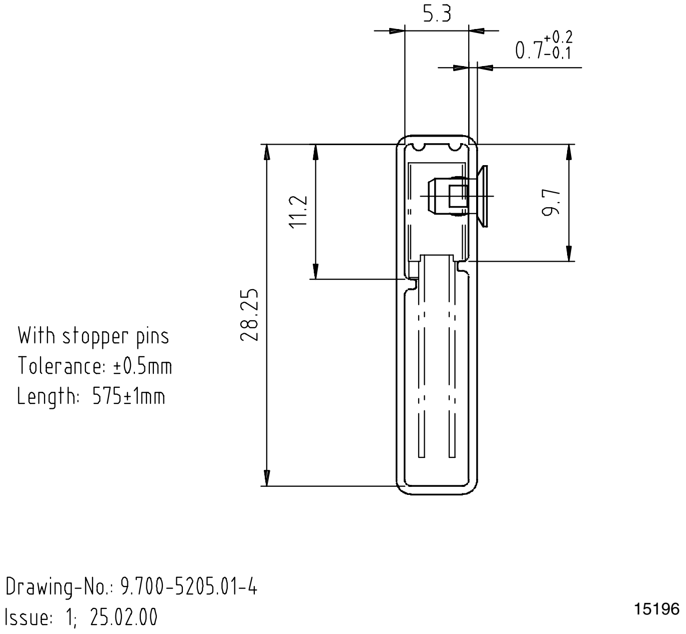

5.3
0.7 +0.2 −0.1
11.2
9.7
28.25
With stopper pins
Tolerance: ±0.5mm
Length: 575±1mm
Drawing-No.: 9.700-5205.01-4
Issue: 1; 25.02.00
15196

Fig. 6

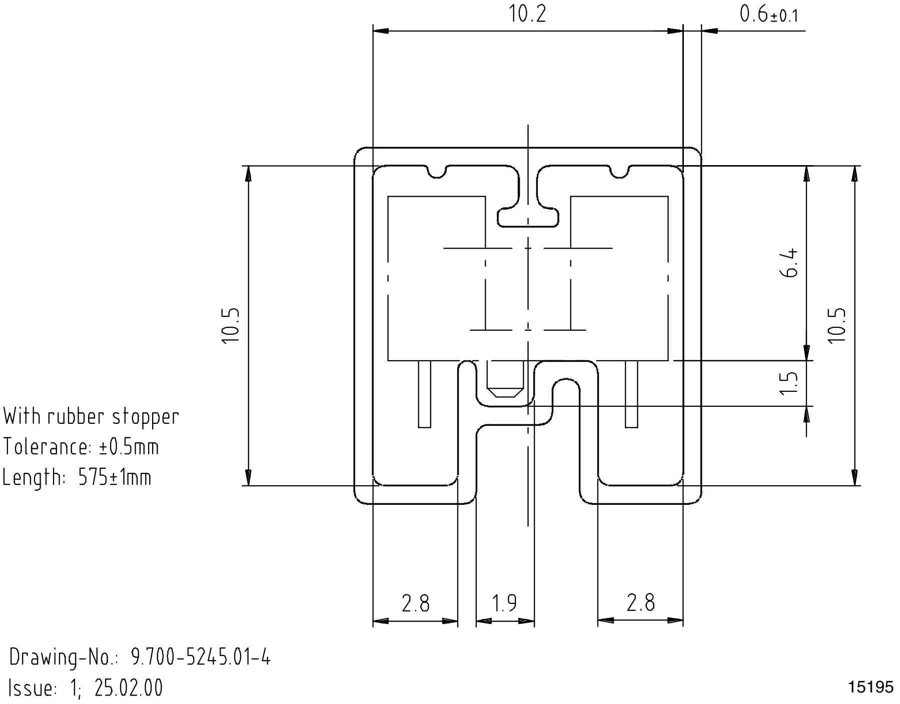
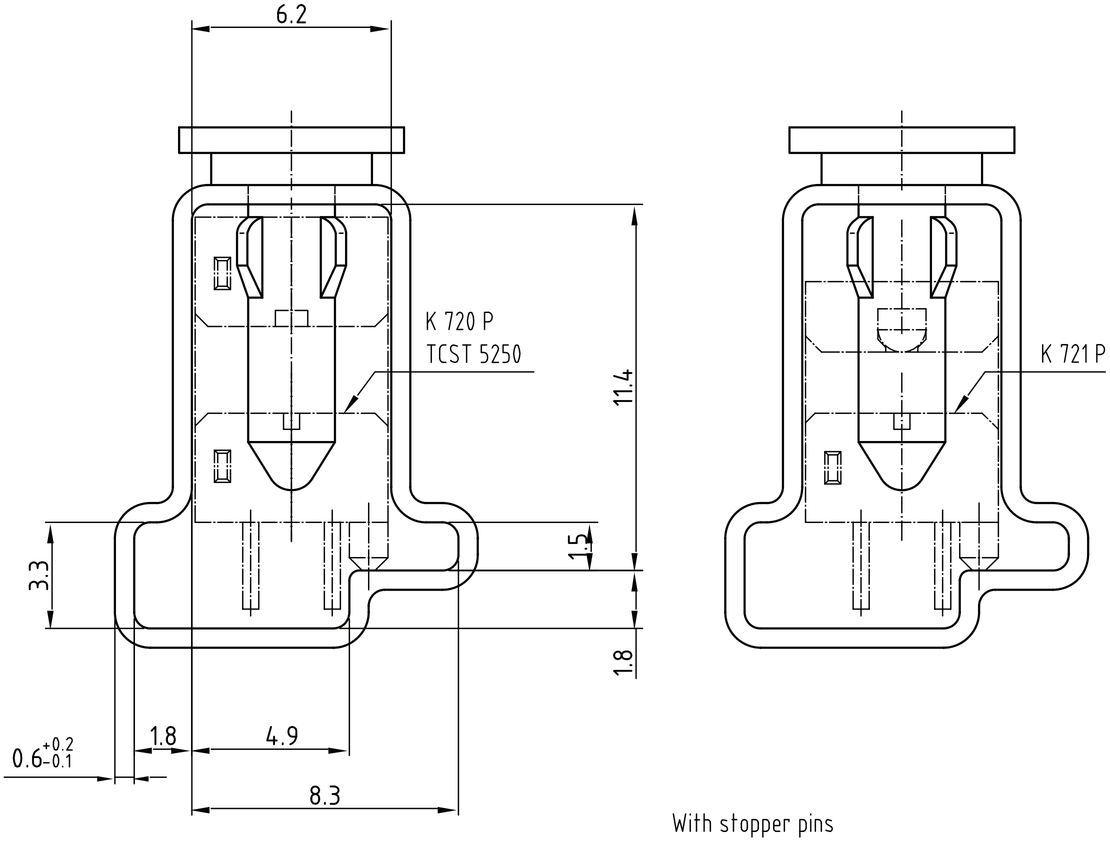

10.2
0.6±0.1
10.5
6.4
10.5
1.5
With rubber stopper
Tolerance: ±0.5mm
Length: 575±1mm
2.8
1.9
2.8
Drawing-No.: 9.700-5245.01-4
Issue: 1; 25.02.00
15195

Fig. 7



Drawing-No.: 9.700-5222.01-4
Issue: 2; 19.11.04
20257

With stopper pins
Tolerance: ±0.5mm
Length: 450±1mm
All dimensions in mm

Fig. 8

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